Page No... 1 P13EE56

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## P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Fifth Semester, B.E. - Electrical and Electronics Engineering **Semester End Examination; Dec. - 2015** 

**Operational Amplifiers and Linear Integrated Circuits** 

<ul> <li>Note: i) Answer FIVE full questions, selecting ONE full question from each unit.</li> <li>ii) Missing data may suitably assume.</li> <li>iii) Use of resistor and capacitor standard values list and op-amp data sheets are permitted.</li> <li>UNIT - I</li> <li>a. Explain the working of a high input Impedance capacitor coupled voltage follower circuit, with a neat circuit diagram.</li> <li>b. Design a High Z<sub>in</sub> capacitor – coupled non inverting amplifier to have a low cut off frequency of 200 Hz. The input and output voltages are to be 15 mV and 3 V respectively and the minimum load resistance is 12 kΩ. Design using a BIFET Op-amp.</li> <li>c. A capacitor coupled voltage follower is to be designed to have a lower cut-off frequency of 120 Hz. The load resistance is 8.2 kΩ and the op-amp used has a maximum input bias current of 600 nA. Design suitable circuit.</li> <li>2 a. Sketch the circuit of a capacitor coupled inverting amplifier using a single polarity power supply. Briefly explain its operation.</li> <li>b. Design capacitor coupled inverting amplifier using op-amp 741, to have voltage gain of 100. Assume signal voltage of 10 mV and load of 4.7 kΩ and f<sub>L</sub> = 120 Hz.</li> <li>c. Explain the upper cut off frequency of an op- amp circuit and derive the condition to set upper cut-off frequency for an Inverting amplifier.</li> <li>UNIT - II</li> <li>3 a. Define slew rate and derive an expression for maximum peal value of a sine wave O/P voltage.</li> <li>b. Discuss operational amplifier circuit stability and show how feedback in inverting amplifier can produce instability.</li> </ul>
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c. Calculate the minimum rise time and maximum undistorted output pulse amplitude at that rise time for an amplifier with closed loop Gain 50, using a 741 op-amp.
a. Sketch the circuit of lag compensating network. Explain its operation. Show how it affects the frequency response of op-amp.
b. List the precautions that should be observed for operational amplifier circuit stability.

P13	EE56 Page No 2	
c.	Explain the effects of:	8
	i) Stray capacitance ii) Load capacitance on circuit stability.	8
	UNIT - III	
5 a.	Draw an op-amp sample and hold circuit sketch the signal, control and output voltage waveforms and explain the circuit operation.	12
b.	Using a BIFET op-amp, design a dead zone circuit to pass only the upper IV portion of the positive half cycle of a sine wave input with a 3 V peak value. Supply voltage is if $\pm$ 15 V.	8
6 a.	Draw the circuit of a Triangular / Rectangular waveform generator which has frequency and duty cycle controls. Show all waveforms and explain the circuit operation.	10
b.	With a neat circuit diagram, explain the operation of precision pulse/minus clipping circuit using two dead zone circuits and show the wave forms at different points.	10
	UNIT - IV	
7 a.	Draw the circuit of second order low and high pass filters and explain the circuit operation.	6
b.	Sketch the circuit of Monostable multivibrator. Draw the input and output waveforms and explain the circuit operation.	8
c.	Design a single stage band pass filter, to have unity voltage gain and a pass band from 300 Hz to 30 kHz. [Assume $C_2 = 1000 \text{ pF}$ ].	6
8 a.	What is a Band pass filter? Sketch the circuit of a single stage band pass filter, explain the low pass and high pass operation of circuit. Discuss the design.	8
b.	Using a 741 op-amp, design the first order active low-pass filter to have a 1.2 kHz cut-off frequency. [ $V_i = 70 \text{ mV}$ ], given.	6
c.	Design an Inverting Schmitt trigger circuit to give triggering points of $\pm$ 2 V. Using a 741 opamp with $V_{cc} = \pm$ 12 V.	6
	UNIT - V	
9 a.	Write a short notes on:	
	i) Universal achieve filter.	12
	ii) Switched capacitor filter.	
b.	With a net circuit diagram, explain the operation of a precision voltage regulator.	8
10 a.	What is phase - locked - loop? Explain it with a block diagram.	8
b.	Sketch the circuit of a voltage follower regulator and explain its operation.	6
c.	Explain the terms:	
		6

Line Regulation, Load Regulation and Ripple Rejection for a d.c. Voltage Regulator.