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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. – Electronics and Communications Engineering

Semester End Examination, Dec-2014

FET and Op – Amp Circuits

Time: 3 hrs *Max. Marks: 100*

***Note** : i) Answer **FIVE** full questions, selecting **ONE** full question from each Unit.*
ii) Assume suitably missing data if any.

Unit - I

1 a. With a neat sketch explain current – voltage characteristics of an n – channel enhancement type MOSFET. Also write the large signal equivalent circuit model of an n – channel enhancement MOSFET operating in the saturation region. 9

b. Explain how MOSFET is used as a switch. 5

c. Design a circuit of Fig. 1(c) so that the transistor operates at $I_D = 0.4$ mA and $V_D = 0.5$ V. The NMOS transistor has $V_t = 0.7$, $\mu_n C_{ox} = 100\ \mu A/V^2$, L = 1 μm and ω = 32 μm, $V_{DD} = 2.5$ V and $V_{SS} = -2.5$ V. Neglect the channel length modulation effect. 6

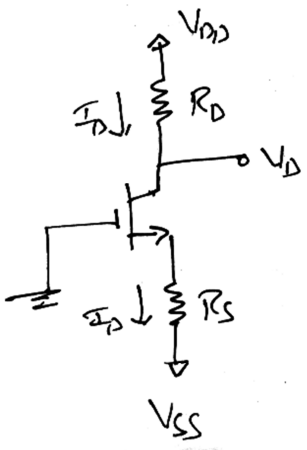

Fig 1(c)

2 a. Explain the purpose of biasing. Discuss biasing using constant current source. 10

b. Discuss high frequency response of the common source amplifier. 10

Unit - II

3a. Define the following terms with respect to Op-Amp. 8
(i) CMRR (ii) PSRR (iii) Input offset voltage (iv) Output impedance.

b. Sketch an illustration to show the effect of op-amp slow rate and explain. State a typical op – amp slow rate. 6

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c. Design a non – inverting amplifier of voltage gain A_V = 66 and V_{in} = 15 mV using 741 op – amp. 6

4 a. Draw a circuit for a differential input / output amplifier. Explain the circuit operator and derive an equation for voltage gain. 10

b. Briefly explain a high input impedance capacitor coupled voltage follower. 10

Unit - III

5 a. Explain the capacitor – coupled difference amplifier with relevant circuit diagram. 6

b. With a neat circuit diagram explain phase – lag compensation technique of frequency compensation. 8

c. What are the effects of slew rate on
(i) Bandwidth (ii) Output amplitude (iii) Output pulse rise time. 6

6 a. What precautions should be observed for Op – amp circuit stability? Draw the necessary diagram. 8

b. Design a voltage source with Zener diode as a reference voltage to provide an output of 9 V to a 500 Ω load. The available supply is ± 12V. Take V_z = 4.5 V and I_z = 20 mA 7

c. With circuit diagram explain the working of current amplifier. 5

Unit - IV

7 a. Design an inverting Schmitt trigger circuit for the following specification V_{cc} = ± 12 V trigger point = ± 2 V. 8

b. With a neat circuit diagram explain the circuit operation of Integrating circuit. 6

c. What is limiting circuits? Explain. 6

8 a. Design a precision full – wave – rectifier to provide 2 V peak output from a sine – wave input with a peak value of 0.5 V and frequency of 1 MHz. 10

b. With a neat sketch explain the working operation of sample and hold circuits. 10

Unit - V

9 a. With a net circuit diagram and waveform explain operation of triangular / rectangular waveform generator with frequency and duty cycle. 10

b. Design a second – order high – pass filter to have a cut–off frequency of 12 kHz. 10

10 a. Define and explain the following terms as applied to voltage regulator.
i) Line regulation ii) Load regulation iii) Ripple rejection. 6

b. Explain voltage follower regulator with relevant circuit diagram. 8

c. List and briefly explain the characteristics of three terminal IC regulators with standard representation of the same. 6

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