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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. – Electronics and Communications Engineering

Semester End Examination; Dec. – 2014

Digital Circuit Design

Time: 3 hrs *Max. Marks: 100*

***Note** : i) Answer **FIVE** full questions, selecting **ONE** full question from each Unit.*
ii) Assume suitable missing data if any..

Unit - I

1 a. With the help of circuit diagram explain the operation of
i) 2 input CMOS NAND gate ii) 2 input CMOS NOR gate. 8

b. Explain with diagram the operation of 2 input TTL NAND gate. 7

c. Explain the following terms with respect to gates.
i) Output switching time ii) Fan-out and Fan-in. 5

2 a. Explain with the help of circuit diagram the operation of
(i) 2 input NMOS NAND gate ii) 2 input PMOS NOR gate. 8

b. Explain the construction and operation of;
i) NMOS enhancement – mode FET ii) PMOS enhancement mode FET 12

Unit – II

3a. Design a combinational logic circuit with 4 inputs a, b, c, d and one output f, which goes high whenever LSB of input or MSB of input is high. Implement using two level basic gates structure. 7

b. Write the Boolean expression for the schematic shown in fig. 1. 5

c. Obtain minimal SOP and minimal POS expression for the function
$f(a,b,c,d) = \bar{a}\bar{b}d + bcd + a\bar{b}d + b\bar{c}\bar{d}$ using K-map. 8

4 a. Find all the prime implicants for the following function using Quine – Mccluskey method.
$f(a,b,c,d) = \pi M(0,2,3,4,5,12,13) + \pi d(8,10)$ 12

b. For the function $f(a,b,c,d) = \sum m(3,4,5,7,8,11,12,13,15)$ obtain minimal product and minimal sum using MEV method. 8

Unit - III

5 a. Explain the working of look ahead carry adder derive the equation for sum and carry. 10

b. Design and implement using basic gates 2 bit magnitude comparator. 10

Contd…2

6 a. Implement full adder and full subtractor using multiplexer. 10

b. Implement the following functions using a single 3 to 8 line decodes and external gates.

$f_1(a,b,c) = \pi M(2,3,4,5,7)$

$f_2(a,b,c) = \pi M(0,2,4,6,7)$ 10

Unit - IV

7 a. Explain how S-R latch can be used as key denouncer. 6

b. Obtain the characteristics equation for SR, JK, D and T flip flop using K – map. 8

c. Draw the circuit of basic bistable element and explain its operation. 6

8 a. With the help of neat diagram explain the working of master slave SR FF. 8

b. What is edge triggering? Explain the working of +ve edge triggered D – FF 6

c. Draw the output waveform for a gated SR Latch, if S, R and clock inputs are as shown in Fig. 2. 6

Unit - V

9 a. Design a 4 – bit register using +ve edge triggered D – FF to operate as per the following table.

Mode select		Register operation
S_1	S_0	
0	0	Hold
0	1	Clear
1	0	Complement the content
1	1	Circular shift register

8

b. Design a mod – 77 synchronous counter by cascading two 4 bit binary counter. 8

c. Construct a 4 bit ring counter using a universal shift register. 4

10 a. Design a synchronous mod – 6 counter using clocked JK – FF. 10

b. Construct the excitation table, Transition table, State table and State diagram for the Moore sequential circuit shown in Fig. 3. 10

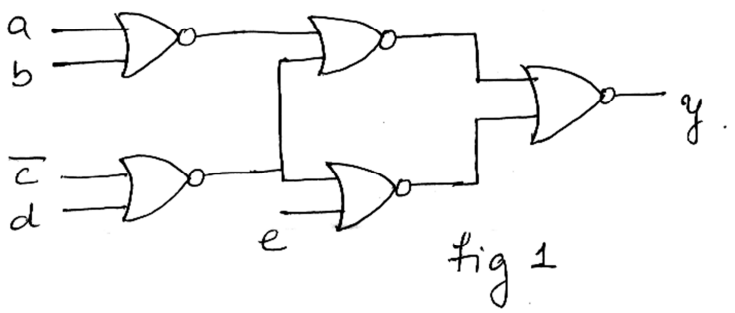

fig 1

Contd…3

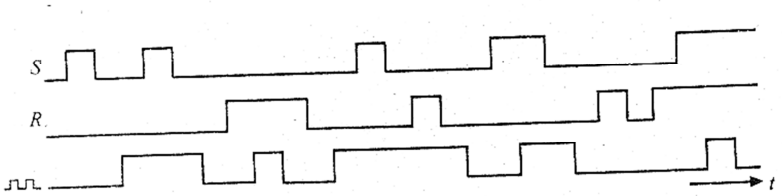

fig 2

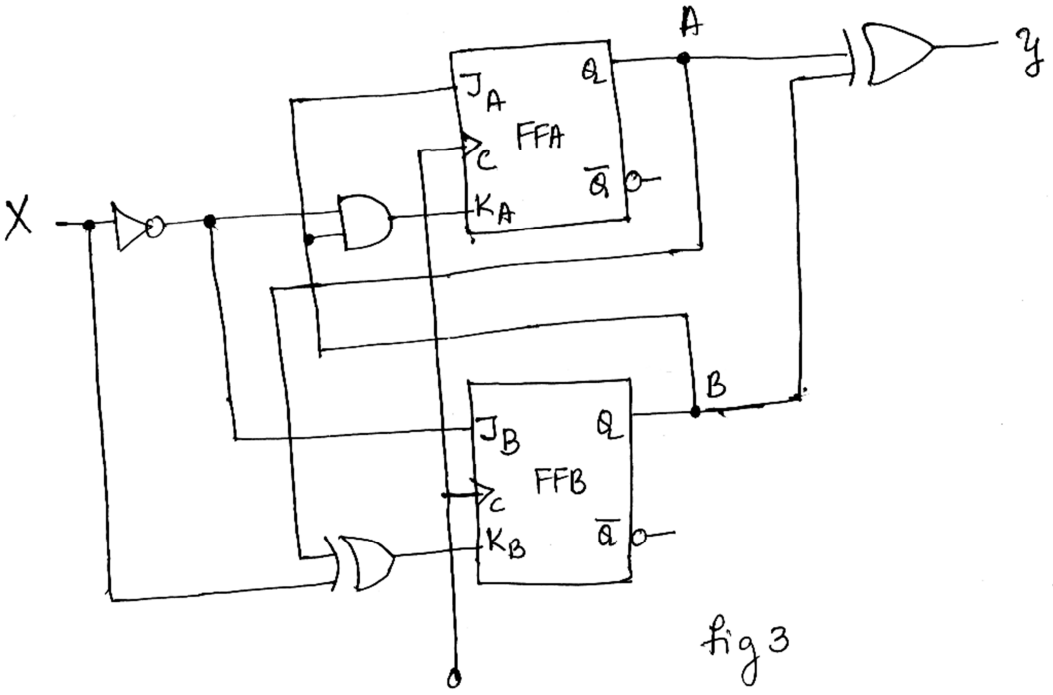

fig 3

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