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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Dec. - 2015

Digital Circuit Design

Time: 3 hrs *Max. Marks: 100*

***Note**: i) Answer **FIVE** full questions, selecting **ONE** full question from each **unit**.*
ii) Assume suitably the missing data if any.

UNIT - I

1 a. For a family of logic components, V_{IL} is 0.6 V and V_{IH} is 1.2 V. What voltages are required for V_{OL} and V_{OH} to provide a noise margin of 0.2 V? — 4

b. Explain the structure and operation of n-channel depletion type MOSFET. — 8

c. Draw the circuit diagram of two-input ECL Nor gate and briefly explain its operation. Mention the advantages and disadvantages of current mode logic. — 8

2 a. Draw the circuit (Schematic) diagram of two-input CMOS AND gate and explain its operation. — 10

b. Draw the circuit diagram of NMOS NAND gate and PMOS NOR gate with truth tables. — 10

UNIT - II

3 a. Simplify the following Boolean expressions using K-map Method,
f(v, w, x, y ,z) = Σm (0, 1, 2, 3, 6,7, 11, 15, 16, 17, 19, 23, 27, 31) — 10

b. Simplify the following Boolean expressions using K-map,
(i) *f(w, x, y, z)* = π(1,2,3,4,9,10)+d(0,14,15) — 5
(ii) *f(w, x, y, z)* = Σm(0,1,2,4,5,9,12) — 5

4 a. Simplify the following Boolean function using QMC method,
f(a, b, c, d) = Σm(0, 1, 2, 8, 10, 11, 14, 15) — 10

b. A comparator compares two numbers A and B of two bit each. Obtain the expression for A>B using MEV technique, considering LSB of B as the MEV. — 10

UNIT - III

5 a. Construct a 5-to-32 line decoder with four 3-to-8 decoder/de-multiplexer and a 2-to-4 line decoder/de-multiplexer Y. Use block diagram construction. — 10

b. Design and implement a combinational logic circuit for Excess-3 to BCD code conversion. — 10

6. a. Implement the following Boolean function,
f(w, x, y, z)=Σm(4,5,7,8,10,12,15) Using 4:1 line multiplier and external gates if, *y* and *z* are connected to select lines S_1 and S_0 respectively. — 8

Contd…..2

b. Construct 32:1, multiplexer using 16:1 multiplexer and 2:1MUX 6

c. Develop the condensed truth table for 4-to-2 line encoder with a valid output where the highest priority is given to the least input with lowest index and obtain the minimal expression for the outputs. 6

UNIT - IV

7 a. Explain the gated JK latch with truth table and explain one of the applications of clocked R S flip-flop. 10

b. Give the logic diagram, truth table and explain the operation of Master-slave RS flip-flop and also derive an expression for characteristic equation. 10

8 a. Draw the logic diagram of Negative Edge triggered D-flip-flop, write its truth table and explain its operation. 10

b. Explain with timing diagram, the concept of set-up time; hold time and propagation delay with respect to negative edge triggered D-flip-flop. 10

UNIT - V

9 a. Realize a 4-bit universal shift register and explain PISO, PIPO, SISO and SIPO. 10

b. Design and implement Mod-16 synchronous counter edge triggered JK flip-flop and draw the wave form. 10

10a. Design and realize a decode counter (Asynchronous) using edge triggered T-flip-flop and draw the waveform. 8

b. Explain the serial binary adder as a Moore network. Obtain the state diagram also. 12

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