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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Fifth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Dec. - 2014

VLSI Circuits and Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer any **FIVE** full questions selecting at least **TWO** full questions from each part*

PART - A

1. a. With the help of a layout, explain the bonding pad frame for interfacing. 6

   b. Bring out the differences between AOI and OAI logic with suitable example. 6

   c. Obtain the block diagram of control of binary words using clocking planes for
   (i) Clocked adder (ii) Clocked ALU. 8

2. a. Determine the resistivity of a sample doped with 10^{15}/cc (P-type) with $\mu_n = 1350\ cm^2/V-\sec$ $\mu_p = 450\ cm^2/V-\sec$ and $n_i = 1.45\times10^{10}\ /\ cc$ 4

   b. Obtain the CMOS schematic and layout for the function $f = \overline{AB+C}$ 4

   c. With relevant cross sectional structure. Explain the formation of nFET and PFET in η-well CMOS technology using self- aligned gate process. 12

3. a. Discuss the latch up phenomenon in η-well CMOs process with cross sectional structure, equivalent circuit and behavioural response curve. 10

   b. Obtain the CMOs schematic and layout of Vertical mount NAND 2 gate. 4

   c. Discuss the design hierarchy at different levels in a CMOS structure. 6

4. a Calculate drain current with $V_{DS} = 2V$, $t_{ox} = 10\ nm$, $\mu_n = 520\ cm^2/V-\sec$, $\left(W/L\right) = 8$, $V_{Tn} = 0.7\ V$ 10

   b. Using RC model, Obtain an expression of resistance of an nFET. 6

   c. With equivalent model, discuss the various capacitance associated with ηFET. 4

PART - B

5. a. Calculate the midpoint voltage of a CMOS inverter for the following data (i) $\beta_n = \beta_p$ (ii) $\beta_n = 2.33\beta_p$, $K_n^1 = 140\ \mu A/V^2$, $V_{Tn} = 0.7\ V$, $K_p^1 = 60\ \mu A/V^2$, $V_{Tp} = -0.7\ V$, $V_{DD} = 3.0\ V$ 6

   b. Starting from the fundamental derive an expression for maximum signal frequency of CMOS inverter. 8

   c. Obtain an expression for power dissipation in terms of activity factor in an inverter and hence obtain the activity coefficients for NAND 2 and NOR 2 6

Contd…2

6 a. Design a non-inverting chain with respective trans conductance for the following data. $C_L = 10\,pF, C_{in} = 20\,fF$ *and* $\beta_1 = 200\,{}^{\mu A}/_{V^2}$ — 8

b. Obtain the schematic of C^2MOS NAND 2 and C^2 MOS NOR2 gate. — 4

c. Discuss the general structure of CVSL logic and hence obtain the schematic of CVSL AND/NAND and CVSL OR/NOR. — 8

7 a. Calculate the resistance and capacitance associated with a line of 225 μm length, 0.35μm, wide, 0.7μm. Thick with $T_{OX} = 0.9\mu m, \quad R_S = 0.02\Omega$ — 8

b. With the help of physical structure and RC model discuss the lumped element coupling circuit model. — 6

c. Analyze the floor planning and routing of sliceable floorplan (block diagram approach). — 6

8 a. Obtain the schematic of 4-bit shift register and charge leakage in shift register. — 7

b. Discuss the timing analysis using basic pipelined stage. — 7

c. Explain the working of basic clock stabilization network. — 6

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