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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Fifth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Dec. - 2015

VLSI Circuits and Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each **unit**.*

UNIT - I

1 a. Explain the following with equations : 7

i) Channel length modulation ii) Substrate bias effect

b. Derive the equation threshold voltage of a MOS structure. 7

c. A PMOS transistor was fabricated on a n-type substrate with a bulk doping density of $N_D = 10^{16}$ cm^{-3}, gate doping (n-type poly) of $N_D = 10^{20}$ cm^{-3}, $\frac{Q_{ox}}{q} = 4\times10^{10} cm^{-2}$ and gate oxide thickness of $t_{ox} = 0.1$ μm. Calculate the threshold voltage at room temperature for $V_{SB} = 0$. Use $\in_{si} = 11.7\in_0$. 6

2 a. Explain the different region of operation for a CMOS inverter. 5

b. Discuss the enhancement load nMOS inverter and depletion load nMOS inverter. 8

c. Consider a CMOS inverter with the following parameters nMOS $V_{TO,\ n}$= 0.6 V, $\mu_n C_{ox}$ = 60 μA/V^2, $(W/L)_n = 8$ pMOS $V_{TO,\ p}$ = - 0.7 V, $\mu_p c_{ox}$ = 25 μA/V^2, $(W/L)_p = 12$, R_L = 10 kΩ. Calculate the noise Margin's and the switching threshold (V_{th}) of this circuit. The power supply voltage is V_{DD} = 3.3 V. 7

UNIT - II

3 a. Explain CMOS Ring oscillator circuit. 5

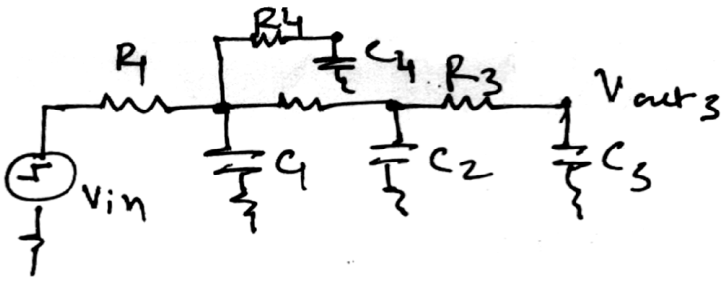
b. Analyze the design of CMOS inverter with delay constraints. 8

c. CMOS inverter with a power supply voltage of V_{DD} = 5 V, determine the fall time τ_{fall}, which is defined as the time elapsed between the time point at which $V_{out} = V_{90\%}$ = 4.5 V and the time point at which $V_{out} = V_{10\%}$ = 0.5 V. Use both the average current method and the differential equation method for calculating τ_{fall}. The output load capacitance is 1 pF. The nMOS transistor parameters are given as $\mu_n C_{ox}$ = 20 μA/V^2, $(W/L)_n = 10$, $V_{T,\ n}$ = 1.0 V. 7

4 a. With a neat diagrams discuss the inter connect capacitance estimation. 7

b. Analyze the interconnect with RC delay model. Use Elmore formula to calculate the delay of given circuit between nodes V_{out3}. 7

Contd…..2



c. Explain the following : 6

i) Power Meter Simulation (ii) Power Delay Product.

UNIT - III

5 a. Explain the generalized NOR structure with multiple inputs with relevant equations. 7

b. Sketch the CMOS logic circuit for the function, 5

$Y = \overline{A(B+C)+D}$

c. Discuss the working of CMOS transmission gates Design 4:1 MUX using TG. 8

6. a. Discuss the clocked NOR SR latch with AOI based implementation and waveform. 8

b. Explain the function of a SR latch using NOR2 gates with gate level schematic and CMOS circuit. 6

c. Describe the function of a CMOS implementation of the D-latch. 6

UNIT - IV

7 a. Discuss the voltage Boot trapping with relevant equations. 10

b. Define pass transistor. Describe how does logic '0' transfer and logic '1' transfer takes place in pass transistor. 10

8 a. Explain the following : 8

i) Zipper CMOs circuits ii) NP- Domino logic

b. Explain the principle of charge sharing with example. 5

c. Explain the dynamic domino CMOS logic with advantages. 7

UNIT - V

9 a. Describe the structure and working of BICMOS inverter circuit. 7

b. Develop the Expression for forward and Reverse active mode of BJT. 8

c. Consider a logic gate for the Boolean function $Z = \overline{(A+B+C).(D+E)}$ design a BICMOS circuit for the function. 5

10 a. Explain latch-up in CMOS inverter. 6

b. Discuss the operation of output circuit and $L\left(\frac{di}{dt}\right)$ noise. 7

c. Explain the following : 7

i) H-Tree Clock distribution ii) Three level buffered clock distribution

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