P13EC52 Page No... 1

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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Fifth Semester, B.E. - Electronics and Communication Engineering Semester End Examination; Dec. - 2015 **Digital Signal processors and its Applications**

Tin	ne: 3 hrs Max. Marks: 100	
Note	: Answer FIVE full questions, selecting ONE full question from each unit .	
	UNIT - I	
1 a.	List the important computational blocks needed on Digital Signal processor and discuss the impact of each of these on the performance.	8
b.	Show that Full address could be used in design of parallel multipliers and further design an 8-bit parallel multiplier using full address.	12
2 a.	Discuss the need for hardware shifters in DSP. Design a 6-bit barrel shifter which can left shift the data.	10
b.	Highlight important features of Indirect addressing method as applicable to Digital signal processors. Explain the circular addressing mode and its utility in digital signal processing.	10
	UNIT - II	
3 a.	Differentiate between parallelization and pipelining. Explain the pipeline operation in TMS320C54 XX processors considering a suitable example.	10
b.	Evaluate the following program snippet writing comments for each instruction operation given in initial values as. $(0200h) = 25h$; $(0210h) = 40h$;	
	SSBX SXM	
	STM #0200h, AR2	
	STM # 0210h, AR3	10
	MPY * AR2+, * AR3+, A	
	STL A, *AR2+	
	STH A, * AR2	
	Find the contents of different data memory location and Auxiliary register.	
4 a.	Draw the functional diagram of CPU of TMS320C54 XX processor and list its highlighting features.	8
b.	List the addressing modes used in TMS320C54XX processor. If AR2, AR3 and AR0 has 0200h, 0250h and 10h respectively. Determine contents of there auxiliary registers after each of the following operation and explain the operation.	

12

- (ii) ADD * +AR2, *AR3-
- (iii) ADD * AR2-, AR3-
- (iv) ADD * AR2-0, * AR3+0

UNIT - III

5 a.	Write an Assembly language program in TMS 320C54xx to determine,	
	y(n) = h(0)x(n) + h(1)x(1) + h(2)x(n-2) + h(3)x(n-3), where h's are coefficients in	10
	Q15 format and \underline{x} 's are input samples in integer format. Use indirect method of addressing and do not use MAC instruction.	10
b.	Draw the general butterfly computation structure and device necessary equation used in computation of the butterfly. Show that multiplying each input variables by 0.414 will avoid overflow.	10
6. a.	Draw the signal flow graph for 8 - point DIT-FFT algorithm, explain the computational structure of a general butterfly with necessary computing equation.	10
b.	Define PID controller and explain its operation. Derive and draw the signal flow graph of PID controller implementation.	10
	UNIT - IV	
7 a.	Design the interface logic which interfaces 8k x 8 program ROM's to the TMS 320C5416 processor in the address range 7FE000-7FFFFFh. The C5416 processor has 23 bit address bus and 16-bit data bus.	8
b.	Discuss the Interrupt handing mechanism in C54XX processor with necessary flow chart.	6
c.	Draw the block diagram of McBSP of TMS320C54XX processor and list its high lighting features.	6
8 a.	Define CODEC. Develop the procedure as an assembly language program to initialize the McBSP 2 for use with PCM 3002 Codec. Comment every line of the code.	10
b.	Differentiate between normal and DMA transfer of Data. List the different parameters to be initialized in DMA operation and explain Register sub addressing technique of configuring DMA.	10
	UNIT - V	
9 a.	Draw the neat block diagram of clipping auto correction pitch detector and explain the role of each block unit.	10
b.	Draw the block diagram of JPEG encoder and decoder and explain the role of the DCT in this approach.	10
10 a.	Enumerate the role of DSP processor in position control system for a hard disk drive with a neat block diagram.	6
b.	Explain the scheme used in measurement of power using DSP processor. How is analog data interfaced to DSP CS402 processor?	8
c.	Show the utility of pulse position modulation (PPM) in encoding of single and multiple biomedical signals with relevant diagrams.	6