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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Sixth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; June/July - 2015

Design and Synthesis Using Verilog HDL

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer any **FIVE** full questions, selecting at least **TWO** full questions from **each part**.*

PART - A

1 a. Declare the following variables in Verilog :

(i) A memory 'M' containing 64 words of 8 bits.

(ii) A 16-bit vector register called 'r' 4

(iii) A two dimensional array (4X4) 'A'

(iv) A parameter 'P'

b. Explain the different system tasks with example. 8

c. Explain number specifications in Verilog with example. 8

2 a. Write a Verilog module for a 4-bit adder using 'for-loop' statement. 8

b. Write a Verilog module for a 16:1 mux using two 8:1 in structural style. 8

c. Explain rise and fall delays in the gate level design with example. 4

3 a. Write a Verilog module that divides the signal 'clk' of 1 MHz by 1 MHz to obtain 1 Hz. Assign the divided signal to net clk 1. 4

b. Explain the following with an example :

i) Relay based timing control

ii) Continuous assignment and implied continuous assignment with an example. 9

iii) Blocking and non-blocking assignment statements with examples.

c. Explain sequential and parallel blocks with an example. 7

4 a. Write a function to perform the following :

i) Parity calculation of a 32 bit value assumes even parity. 8

ii) Left/Right shifter of 32-bit value.

b. Define a module called full adder built from two half adders. The module should contain the task half adder. 8

c. Write a Verilog module for a full adder using case statement. 4

PART - B

5 a. Explain the usage of $ setup, should and $ width system task. 6

b. Write the switch level Verilog description of NAND Gate and NOR gate. 6

Contd…2

	c.	With a neat block diagram explain the various steps in the flow that use delay back annotation	8
6	a.	Write the description of a T-flip flop as a sequential UDP and show how it can be used in the 4-bit ripple counter.	8
	b.	Write the uses of Programming Language Interface (PLI).	6
	c.	Write the PLI routine to monitor Nets for value charges.	6
7	a.	Explain basic computer aided logic synthesis process with flow chart.	5
	b.	Design 16-bit ALU using 4-bit ALU's by Horizontal partitioning and Vertical partitioning techniques.	10
	c.	Write a note on functional verification.	5
8	a.	Write a code for RTL description for newspaper vending machine FSM.	10
	b.	Explain the functional verification flow environment.	10

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