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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Sixth Semester, B.E. – Electronics and Communication Engineering

Semester End Examination; June - 2016

Analog CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Plot the On-resistance of an n-channel MOSFET as a function of V_G , with drain open, source connected to IV supply. Assume $\mu_n c_{ox} = 50\,\mu A/V^2$ w/L = 10 $V_{Th} = 0.7\,V$ — 6

b. Discuss the second order effects. — 8

i) Channel length modulation ii) sub threshold conduction

c Analyze the MOS device capacitances along with fabrications structure. — 6

2 a. Obtain the small signal equivalent circuit of source follower. Hence plot voltage gain versus input voltage. — 6

b. Along with I/O characteristic, explain the working of common – gate amplifier. — 6

c. Explain the working of cascade stage along with I/O characteristics. — 8

UNIT - II

3 a. Discuss the noise reduction by differential operation with necessary arrangement. — 6

b. Show that $|A_v| = \frac{4}{3} g_{m1} R_D$ by conducting basic differential pair such that M_2 is twice as wide as M_1 — 6

c. Basic differential pair uses a resistor rather than a current source with tail current of 1mA. Assume $\left(\frac{w}{L}\right)_{1,2} = \frac{2.5}{0.5}$, $\mu_n c_{ox} = 50\mu A/V^2$, $V_{TH} = 0.6\,V$, $\lambda = V = 0$, $V_{Dn} = 3\,V$ — 8

(i) What is the required input CM for which R_{SS} sustains 0.5 V?

(ii) Calculate R_D for a differential gain of 5.

4 a. Discuss the applications of current sources along with schematic diagrams. — 8

b. Using Asymmetric swings in differential pair with active mirror, discuss the circuit for calculations of G_m. — 6

c. Briefly discuss the common-mode properties. — 6

UNIT - III

5 a. Derive an expression for positive- temperature, coefficient voltage along with circuit. — 8

b. Discuss the working of conceptual generation of temperature independent voltage. — 6

c. Discuss in brief the speed and noise issues in Band gap references. — 6

Contd….2

6	a.	Discuss the working of switched capacitor amplifier in sampling and amplification mode.	8
	b.	Explain the working of unity gain sampler/buffer circuit.	6
	c.	Analyze the response of Discrete time integrator to a constant input voltage.	6

UNIT - IV

7	a.	Analyze the working of ring oscillator with 2-pole feedback system. Obtain the loop gain characteristic of the same.	10
	b.	Sketch the open-loop voltage gain and phase of two turned stages in an f/b loop of LC oscillator. Neglect transistor capacitance.	10
8	a.	Analyze the working of Colpitt's oscillator.	10
	b.	Discuss the working of voltage controlled oscillator. Discuss an expression of gain or similarity of the circuit.	10

UNIT - V

9	a.	Analyze the working of frequency-looked loop along with relevant diagram.	8
	b.	Discuss the process of frequency multiplication and frequency synthesis.	12
10	a.	Analyze the conceptual operations of phase/frequency detector along with waveform.	10
	b.	Discuss the skew and jitter reduction of PLL system.	10

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