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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Sixth Semester, B.E. - Electronics and Communication Engineering

Make-up Examination; July - 2016

Digital Design Using Verilog HDL

Time: 3 hrs *Max. Marks: 100*

***Note**: i) Answer **FIVE** full questions, selecting **ONE** full question from each unit.*
ii) Assume missing data suitably.

UNIT - I

1 a. Explain the different system tasks with examples. 8

b. Write a verilog code and stimulus of a SR Latch. 6

c. Describe the port connection rule in a module Installation. 6

2 a. Write a structural description of a 4 bit adder and also write the stimulus for it. 8

b. Define the ;

(i) Rise time

(ii) Full time

(iii) Turn off delay with examples. 6

c. Explain the assignment delay, implicit assignment delay and net declaration delay for continuous assignment statements. 6

UNIT - II

3 a. Describe the event based timing control mechanism using behavioral modeling with examples. 8

b. Explain the sequential and parallel blocks with examples. 6

c. Write a verilog code for a gate level ripple adder using generate statement. 6

4 a. Describe the difference between tasks and functions. 6

b. Write a verilog code for 8 functions of ALU using function, 8

0→ a,	3→ a/b	6→ a >> 1
1→ a+b,	4→ a%1	7→ a > b
2→ a–b,	5→ a << 1	

c. Explain with block diagram of the debugging and analysis of simulation with value change dump (VCD) file. 6

UNIT - III

5 a. Explain the different types of delay models with examples. 6

b. Define system tasks for timing checks and explain with examples. 8

Contd….2

	c.	Draw the schematic of 4 to 1 multiplexer using transmission gate and write a verilog code for the same using switching.	6
6	a.	Briefly discuss the flow diagram of delay back annotation.	6
	b.	List the user defined primitives (UDP) rules of verilog language.	6
	c.	Write a verilog stimulus of 4 to 1 multiplexers with UDP.	8

UNIT - IV

7	a.	Explain the different types of class routine in programming language interface (PLI).	8
	b.	Write the uses of programming language interface (PLI).	6
	c.	Explain how PLI routine is used in a verilog simulation.	6
8	a.	Define logic synthesis and explain the basic computer aided logic synthesis process.	5
	b.	Briefly discuss partitioning techniques to help logic synthesis. Provide the optimal gate level Net list.	7
	c.	Explain the design flow from RTL description for a gate level description.	8

UNIT - V

9	a.	Write a verilog code for RTL description for newspaper vending machine FSM.	10
	b.	Explain the functional verification flow environment.	10
10	a.	Draw the neat diagram and briefly discuss the different ways to stimulate a design.	10
	b.	Explain the formal verification and equivalent checking.	10

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