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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Sixth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; June - 2016

Digital Design using Verilog HDL

Time: 3 hrs *Max. Marks: 100*

***Note**: i) Answer **FIVE** full questions, selecting **ONE** full question from each unit.*
ii) Assume missing data suitably.

UNIT - I

1 a. $ Display is the main system task. Write the display syntax ;
i) to display value of current simulation time,
ii) to display value of port id 5 in binary,
iii) What will happen if there are no arguments in $display? — 4

b. Discuss the following data types :
value sets, nets, registers, vectors. — 8

c. Explain the port connection rules and connecting port to external signal by ordered list and name with example. — 8

2 a. Design and implement a 4x1 multiplexer in structural description. Write the Verilog program and stimulus. — 8

b. Write the dataflow description in Verilog for a 4 bit CLA adder design. — 8

c. i) Use right shift (>>) , left shift (<<),
$Y_1 = X >> 1;$
$Y_2 = X << 1;$
If X = 4'b1100. Find Y_1, Y_2. — 4
ii) Discuss conditional operator (?:).

UNIT - II

3 a. How to initialize memory from file? Discuss with appropriate keywords. Give an example program to initialize memory and read memory file init.dat. — 8

b. Discuss the system tasks to write to files with an example. — 6

c. Illustrate the difference between tasks and functions. — 6

4 a. Explain :
i) Blocking Assignment — 8
ii) Non-blocking assignment applications.

b. Write a recursive functions to obtain the factorial of a number. Use $ display to show the output. — 8

c. Discuss zero delay control. Explain the zero delay control with an example. — 4

Contd…2

UNIT - III

5	a.	Give the delay specification in MOS and CMOS switches.	8
	b.	Discuss the statement specparam, used inside specify block, with an example.	6
	c.	Discuss pin-to-pin delay in path delay modeling with an example.	6
6	a.	Design a 1 bit full adder using instartification of udp primitives. Write the module example program.	6
	b.	Discuss the design of a CMOS inverter and write a program using PMOS and CMOS switch.	6
	c.	Give the UDP definition for the T-flip flop.	8

UNIT - IV

7	a.	Write the consumer routine for VCL example.	6
	b.	Discuss the Access routines in PLI library with example of routine. To get module port list.	8
	c.	Explain logic synthesis process.	6
8	a.	Discuss the technology library and design constraints.	6
	b.	Discuss RTL for magnitude comparator.	10
	c.	Write a note on design partitioning namely vertical partitioning.	4

UNIT - V

9	a.	Draw the finite state machine for newspaper vending machine. Write the RTL description.	10
	b.	Discuss the functional verification environment with components of the environment.	10
10	a.	What is hardware acceleration? Discuss the verification methodology.	6
	b.	Discuss the equivalence checking.	6
	c.	What is structural coverage and functional coverage analysis?	8

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