U.S.N | | | | | | | | | | |

P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Seventh Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Dec. - 2014

ARM Processor

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer any **FIVE** full questions, selecting at least **TWO** full questions from each part.*

PART - A

1.	a.	Explain the memory controllers of Interrupt Controller.	6
	b.	Describe the complete ARM register set with a diagram.	6
	c.	With a diagram, Explain ARM7, ARM 9 and ARM 10 pipeline stages & also describe the pipeline executing characteristics.	8
2	a.	Explain single-Register Transfer and Multiple Register Transfer Instruction with an example for each.	6
	b.	Explain the ARM-THUMB interworking with BX and BLX instruction.	5
	c.	Write an ARM assembly language program to find square of a number using multiplication technique.	5
	d.	Mention the function of the following instruction: i) SWI ii) SWP iii) RSC iv) TEQ.	4
3	a.	Write a C program and corresponding ARM assembly code to unroll the packet checksum loop by four times. Assume that the number of words in the packet N is a multiple of four.	8
	b.	Describe the issues encountered when porting C code to the ARM Code.	8
	c.	Explain ARM-THUMB procedure Call Standard (ATPCS) argument passing with a diagram.	4
4	a	Describe Instruction scheduling and also explain ARM 9 TDM1 operation with a diagram.	10
	b.	Write an assembly code to read or write a 32-bit word using the unaligned address P. Use three scratch register t_0, t_1, t_2 to avoid interlocks.	10

PART - B

5	a.	Write the algorithm and corresponding C code to find the square root of a 32-bit unsigned integer by trial subtraction.	10
	b.	Explain the saturated and rounded Arithmetic operations along with as code.	10
6	a.	Explain how IRQ and FIQ Exception causes the processor hardware to go through a standard procedure.	5
	b.	Mention the different interrupt handling schemes.	5
	c.	With suitable flow diagram, explain Reentrant interrupt handler.	10
7	a.	Explain Sandstone code structure with suitable steps.	10
	b.	With a diagram and code, explain the two stages of context switch.	10
8	a.	Describe the Basic architecture of a Cache memory with a diagram.	6
	b.	Explain the ARM 940T, 64-way set associate D-Cache using a CAM.	7
	c.	Write a C code to initialize the MPU, Caches and write buffer for the protected system.	7