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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Seventh Semester, B.E. - Electronic and Communication Engineering

Semester End Examination; Dec. - 2014

Analog CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer any **FIVE** full questions, selecting at least **TWO** full questions from each part.*

PART - A

1 a. With the help of MOS device capacitance, Explain the variation of gate – source and gate-drain capacitance versus $V_{GS.}$ 8

b. Explain the small signal model for the common source stage with R load for the saturation region along with the necessary equation for $A_{v.}$ 8

c. What is folded cascade? Write the folded cascode circuit with N-MOS input. 4

2 a. With the help of circuit define the Gilbert the Cell. Explain why the Gilbert cell can operate as an analog voltage multiplies. 6

b. Explain the working principle of basic different pair along with the I/O characteristics. 10

c. Mention the advantages of Different circuit over single ended operation. 4

3 a. Explain the modified cascode mirror for low voltage operation using a source follower level shifter. 10

b. Explain the large signal behavior of the differential pair active current mirror along with input-output characteristic. 10

4 a. Derive the output current equation which is independent of the supply voltage along with circuit diagrams. 10

b. Define the following: 5

i) Feedback polarity ii) Band gap reference

c. Explain the generation of PTAT current using a simple amplifier. 5

PART - B

5 a. Explain the switched capacitor amplifier along with sampling mode, amplification mode. 8

b. Explain the response of a sampling circuit to different input level and initial conditions. 6

c. With the help of charge injection circuit, discuss the input/output characteristics of sampling circuit in the presence of charge injection. 6

6. a Define the voltage controlled oscillators and explain the important performance parameter of VCO'S. 12

b. Explain the Colpitts oscillator along with the equivalent circuit wit input stimulus. 8

Contd….2

7 a. Explain the skew and jitter reduction of phase – locked loop system. 10

b. Define phase detector along with its example and explain conceptual operation of phase/ frequency detector. 10

8 a. Explain the short –channel effects with respect to,

i) Threshold of Voltage Variation 10

ii) Effect of velocity saturation of drain current saturation.

b. With the help of performance envelope as a function of process parameters. Explain the process corners. 10

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