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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Seventh Semester, B.E. – Electronics and Communication Engineering

Semester End Examination; Dec. - 2015

Analog CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: i) Answer any **FIVE** full questions, selecting atleast **TWO** full questions from each **part**.*
ii) Assume missing data if any appropriately.

PART - A

1 a. Derive and explain I/V characteristics of MOSFET from fundamental concepts. 12

b. Explain the working of source follower with its I/O characteristic and small signal equivalent circuit obtain expression for g_m and $A_{v.}$ 8

2 a. Explain the operation of basic differential pair with a relevant diagram and I/O characteristics. 8

b. In the circuit shown in Fig. 2(b) M_2 is twice as wide as M_1. Calculate the small signal gain, if the bias voltage of V_{in1} and V_{in2} are equal.

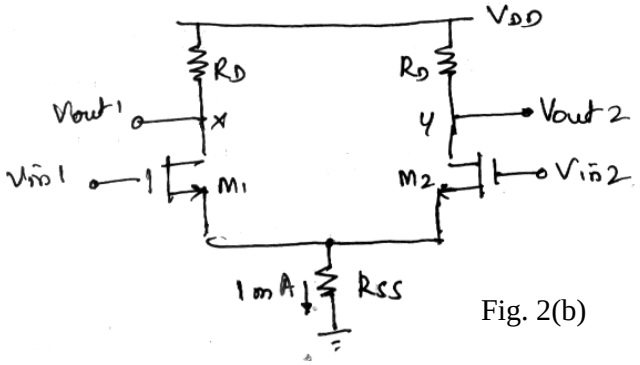

Fig. 2(b) 6

c. The circuit of Fig. 2.C uses a resistor rather than a current source to define a tail current of 1 mA.

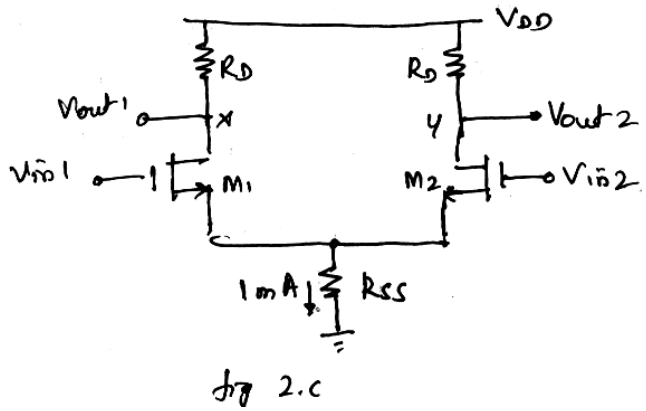

fig 2.c 6

Assume $(W/L)_{1,2} = 2.5/0.5$, $\mu_n C_{Ox} = 50\ \mu A/V^2$, $V_{TH} = 0.6$ V, $\lambda = \gamma = 0$ and $V_{DD} = 3$ V.

i) What is the required input CM for which R_{SS} sustains 0.5 V?

ii) Calculate R_D for a differential gain of 5.

Contd……2

3 a. Discuss the working of cascode current mirror with cascode current source and bias voltage generator. 10

b. Draw the circuit for calculation of G_m and calculation of R_{out} with respect to Active current mirror and derive the respective expressions. 10

4 a. Explain the conceptual generation of temperature independent voltage in the band gap reference and draw the actual implementation circuit of the concept. 12

b. Explain the effect of op - amp offset voltage on the output voltatge of band gap reference and means to overcome the same. 8

PART - B

5 a. Explain the track and hold capabilities of a sampling circuit using MOSFET switch. 6

b. In the circuit shown in Fig. 5 (b), calculate minimum and maximum on – resistance of M_1. Assume; $\mu_n C_{Ox} = 50\ \mu A/V^2$.

$W/L = 10/1$, $V_{TH} = 0.7$ V, $V_{DD} = 3$ V and $\gamma = 0$

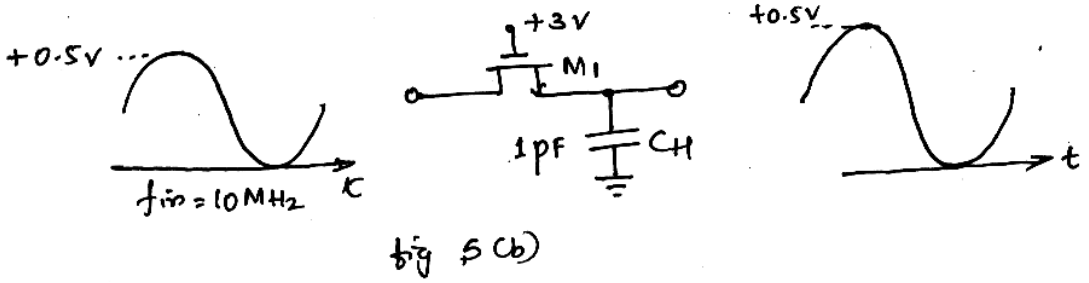

fig 5 (b) 6

c. Explain the unity gain sampler in sampling mode and in amplification mode with relevant diagrams. 8

6 a. Explain the working of crossed coupled oscillator with the help of loop gain characteristics. 10

b. Explain the significance of any five parameters of VCO. 10

7a. Explain the working of a charge pump PLL with relevant circuit diagram and waveforms. 10

b. Explain the process of frequency multiplication and frequency synthesis. 10

8 a. Discuss the short channel effects with respect to,

i) Threshold voltage variation 10

ii) Velocity saturation.

b. Explain level 3 MOS device model along with fabrication structure and respective expressions. 10

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