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## P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

## Seventh Semester, B.E. - Electronics and Communication Engineering Semester End Examination; Dec - 2016/Jan - 2017 Advanced Microcontroller

Time: 3 hrs Max. Marks: 100 *Note*: Answer *FIVE* full questions, selecting *ONE* full question from each unit. UNIT - I 1 a. Draw the functional block diagram of MSP 430 F2013 and explain units used for peripheral 10 functions. b. Discuss structure and mechanism of 'Reset' in MSP 430. 10 2 a. Discuss important features of clock generator of MSP 430. Justify its contribution to low 8 power feature. Discuss different addressing modes of MSP 430 with an example for each. 8 Show the formation of Format-1 instruction. 4 **UNIT - II** 3 a. Discuss the issues associated with interrupts. 8 Identify switch debouncing in push button switch. Discuss role of SR flip flop and RC filter in 8 handling switch debouncing. Show the bias connection for LCD controller to provide bias voltage to drive segments and 4 back planes. 4 a. List the sequence of steps during an interrupt request. Differentiate between subroutine and 6 interrupt service routine. List the different functionality of register associated with port P1 in a MSP 430 F2xx. 6 Discuss the different hardware approaches used to drive a heavier load than the MSP 430 can 8 supply. **UNIT - III** 5 a. Explain typical embedded device based on an ARM core with neat block diagram. 8 b. Discuss pipelining in ARM-7 core with an example. 6 c. Illustrate the following in ARM processor, i) Moving 32-bit constant into a register 6 ii) Moving contents of 'cpsr' or 'spsr' to and from a register. 6 a. Discuss the hardware extension of ARM core. 8

Explain functionalities of memory and interrupt controller in ARM based embedded system.

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| Illustrate with proper ARM instructions:   | 7  |  |  |  |  |  |
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| i) Barrel shifting operation with an example ii) Software interrupting.                    |  |  |  |  |  |  |
| UNIT - IV  |  |  |  |  |  |  |
| a. Highlight the features of thumb instruction with an example to bring out its advantage. |  |  |  |  |  |  |
| Illustrate the advantage of using,   |  |  |  |  |  |  |
| i) Unsigned types over Signed types operations for diversion                               | 8  |  |  |  |  |  |
| ii) 'int' rather than 'char' type for local variables.                                     |  |  |  |  |  |  |
| List the different issues one may encounter when posting C code to the ARM.                |  |  |  |  |  |  |
| a. Discuss the following and provide remedies to avoid it,                                 |  |  |  |  |  |  |
| i) Pointer aliasing ii) Unaligned data and Endianess.                                      | 10   |  |  |  |  |  |
| b. Differentiate thumb stack operation from its equivalent ARM instruction.                |  |  |  |  |  |  |
| Define loop unrolling. List the techniques to write loop efficiently in a program.         | 6  |  |  |  |  |  |
| UNIT - V   |  |  |  |  |  |  |
| a. Discuss the exceptions and associated modes of ARM processor.                           |  |  |  |  |  |  |
| p. Provide flowchart for priority interrupt handling.                                      |  |  |  |  |  |  |
| List the features supported by $\mu HAL$ and Angel.  |  |  |  |  |  |  |
| a. Discuss the mechanism of handling IRQ and SWI exceptions.                               |  |  |  |  |  |  |
| Discuss Nested and Re-entrant handling mechanism with relevant flow diagrams.              | 10   |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  | Discuss the following and provide remedies to avoid it,  i) Pointer aliasing  ii) Unaligned data and Endianess.  Differentiate thumb stack operation from its equivalent ARM instruction.  Define loop unrolling. List the techniques to write loop efficiently in a program.  UNIT - V  Discuss the exceptions and associated modes of ARM processor.  Provide flowchart for priority interrupt handling.  List the features supported by $\mu$ HAL and Angel.  Discuss the mechanism of handling IRQ and SWI exceptions. |  |  |  |  |  |