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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Eighth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; June/July - 2015

Low Power VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: i) Answer any **FIVE** full questions, selecting at least **TWO** full questions from each part.*
ii) Missing data may be suitably assumed.

PART - A

1. a. Derive the expression for surface space charge region and the threshold voltage of the MIs diode. 8

   b. Define the following : 4

   i) Sub threshold swing ii) Submicron MOSFET

   c. Derive the expression for sub threshold current of N channel MOSFET. 8

2 a. Discuss the influence of overlap capacitors and diffusion capacitance in calculation of load capacities along with suitable expression. 8

   b. Mention the five key principles of low power VLSI design. Explain the hierarchy of limits with respect to material and circuit limits along with relevant equation. 12

3. a. Discuss the power optimization using operation reduction through put for the functions. 6

   i) $f_1 = x^3 + Ax^2 + x + C$

   ii) $f_2 = x^2 + Ax + B$

   b. Briefly explain simple data path with an adder and a comparator with respect to Architecture driven voltage swing. 6

   c. Show that n bit comparator circuit using pre-commutation based optimization will minimize area and power. 8

4 a. Obtain the state diagram and state assignment for a state machine that produces on output '1' whenever a sequence of five 1's appear else it outputs a '0'. 8

   b. Mention some of the transistor reordering method with respect to circuit level optimization. Briefly discuss each. 12

PART – B

5 a. List the non clocked types of circuit design style. Briefly discuss each. 12

   b. Define the term; 8

   i) Drain Induced barrier Lowering effect

   ii) Gate Induced Drain Leakage.

   iii) Punch thorough

   iv) Gate oxide tunneling.

Contd…2

6	a.	With a neat block diagram explain the self adjusting threshold voltage schemes (SATS).	6
	b.	Explain with schematic and principles of SSI CMOS inverter along with V – I characteristics.	8
	c.	With a neat schematic, explain the working of a DCVS type voltage level converter.	6
7	a.	Derive an expression for energy dissipation in transistor channel using an RC mode.	10
	b.	Describe the generic resonant scheme for adiabatic clock (Power supply) generation circuits. List some of the problem it.	10
8	a.	With two examples. Explain how to minimize memory access costs.	8
	b.	List the software power estimation techniques. Briefly discuss each.	12

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