U.S.N | | | | | | | | | | |

P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Eighth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; June - 2016

Low Power VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: i) Answer any **FIVE** full questions, selecting at least **TWO** full questions from each part.*
ii) Assume missing data suitably, if any.

PART - A

1. a. Briefly explain the various sources of power dissipation in CMOS VLSI circuits. 6

   b. Derive an expression for the depth of depletion region in the MIS structure, stating clearly the assumptions made. 8

   c. What is gate-induced drain leakage? How is it caused? What are its effects? What are the remedies for the same? 6

2. a. Show that the short circuit power dissipation in an unloaded CMOS inverter is,

$$Psc = \frac{1}{2}.\frac{\beta}{V_{DD}}\left(V_{DD} - 2V_T\right)^3 \frac{\tau}{T}$$

   12

   Clearly state the assumptions made. What is the technique used to reduce this power dissipation?

   b. Briefly explain the various contributors to the load capacitance in a CMOS inverter. 8

3. a. Explain first order difference algorithm for low power design. 7

   b. Describe how power optimization can be achieved using operation reduction. 6

   c. Consider an n-bit magnitude comparator explain how pre-computation logic can be used to reduce power dissipation in it? 7

4. a. Explain with a suitable example how the state encoding of an FSM can be done using the "Likelihood of state transition information. 10

   b. List the four components of circuit optimization algorithms. Explain the following with reference circuit level transform for power optimization, 10

   (i) Gate- delay model

   (ii) Switching event probabilities.

PART - B

5. a. Briefly explain : 10

   (i) Pseudo-nMOS logic (ii) Domino logic.

   b. Explain the various design issues to be addressed in the design deep submicrometer devices. 7

   c. Define aspect ratio (AR) of the submicron device, What is its significance? 3

Contd….2

6 a. Explain the following low-voltage circuit design techniques :
(i) Steeper subthreshold swing
(ii) Multiple threshold voltage. 10

b. How does the use of multiple supply voltages reduce the power dissipation in CMOS circuits? What are the effects of multiple voltage design on IC layout? 10

7 a. With the help of neat diagram explain the design of the buffer chain (reversible logic). Discuss the issues to be addressed. 10

b. Draw the generic resonant scheme for adiabatic clock generation circuits. What are the problems faced with these circuits? 10

8 a. Discuss the following software power estimation techniques :
(i) Gate level power simulation
(ii) Bus switching activity. 10

b. List the objectives to be fulfilled by power minimization techniques related to memory design. 5

c. List the various practices used to minimize memory bandwidth requirements. 5

* * * *