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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. – Information Science and Engineering

Semester End Examination; Dec. - 2014

Digital Design

Time: 3 hrs *Max. Marks: 100*

***Note** : i) Answer **FIVE** full questions, selecting **ONE** full question from each Unit.*
ii) Assume suitable missing data if any.

Unit - I

1 a. With the help of K – map, simplify the given function and get the minimal SOP and POS expression and give the logic circuit using logic gates. 10

$f(A,B,C,D) = \sum m(1,2,3,6,8,9,10,12,13,14)$

b. Write the algorithm for generating prime implicants with a suitable example of your choice. 10

2 a. Prove the following laws :

i) Idempotent ii) involution law

iii) De Morgan's Law iv) Associative law using postulates. 10

b. With an example of your choice explain :

i) 5- variable maps ii) 6 – variable maps. 10

Unit - II

3 a. With neat sketches explain the concept of carry look ahead adder in detail. 10

b. Define encoder, with neat sketches explain 8 – to – 3 line encoder along with its truth table. 10

4 a. Define multiplexer. Explain the concept of 4 – to – 1 line multiplexer along with its logic diagram, truth table and symbol. 10

b. Explain the concept of a 1 – bit comparator along with its truth table and circuit diagram. 10

Unit - III

5 a. Write short notes on the following with relevant circuit diagrams :

i) PLD ii) PLA 10

b. Explain a 2 – bit A/D converter in detail. 10

6 a. Write a note on PROM and PAL. 10

b. Explain the working of a 8 – bit D/A converter using R/2R resistors with suitable sketches. 10

Unit - IV

7 a. Give a clocked JK master slave logic circuit and explain how race around condition is resolved. Give both block diagram using clocked S – R FF and also using only NAND – to – NAND gate network. 10

b. Explain Jhonson counter and sequence generator with suitable circuit diagrams. 10

8 a. Give the diagram of 4 – bit bi directional shift register with parallel load. Explain how shift right, shift left and parallel load can be performed. 10

b. With an example of your choice explain with relevant diagrams and truth tables for the following concepts : 10

i) Ring counter. ii) Sequence detector.

Unit - V

9 a. Design synchronous MOD – 10 up counter using S – R flip flop. Give excitation table of S – R flip flop, state diagram and state table. 10

b. Design a 3 – bit binary up counter using 'T' flip flops with relevant calculations. 10

10 a. Differentiate between mealy model of a clocked synchronous sequential network and Moore model of a clocked synchronous sequential network. 10

b. Explain the following concepts related to sequential circuits:

i) State transition diagram

ii) State synthesis table 10

iii) State reduction technique.

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