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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. – Information Science and Engineering

Semester End Examination; Dec. - 2014

Computer Organization

Time: 3 hrs *Max. Marks: 100*

***Note** : i) Answer **FIVE** full questions, selecting **ONE** full question from each Unit.*
ii) Assume suitable missing data if any.

Unit - I

1 a. Write the basic performance equation and explain its role. 6

b. With block diagram, explain the functional units of computer system 6

c. With block diagram of bus connection for processor, keyboard and display, explain basic input / output organization. 8

2 a. Explain with an example, BIG – ENDIAN and LITTLE ENDIAN assignments. 6

b. Explain shift and rotate instructions with example. 8

c. What is overflow? Perform the following: 6

i) (-06) ii) +06
-(-05) -(-02)

Unit - II

3 a. Explain centralized bus arbitration with neat diagram. 10

b. With a block diagram, explain keyboard to processor connection in parallel port. 10

4 a. What is interrupt? Explain vector interrupt and interrupt nesting. 10

b. Define DMA explain registers in a DMA interface. 4

c. Explain the distributed arbitration, with a neat diagram. 6

Unit - III

5 a. Explain any two mapping functions with respect to cache. 10

b. With neat diagram explain the structure of an SDRAM. 6

c. Explain cache memories. 4

6 a. With the help of diagram, explain the internal organization of bit cells in a memory chip. 10

b. Explain a simple method of translating virtual address of a program into physical address, with the help of a diagram. 10

Unit - IV

7 a. With the help of block diagram, explain the 4 bit carry look ahead adder. 6

b. Multiply – 13 and +11 using Booth's multiplication and bit pair recording. 8

c. Explain the IEEE standard for floating point number representation. 6

8 a. Draw a figure to illustrate a 16 bit carry look ahead adder using 4 bit adder blocks and explain its working principle. 10

b. Draw circuit diagram for binary division. Explain the restoring and non restoring division algorithm with suitable examples. 10

Unit - V

9 a. Explain the process of fetching a work from memory with the help of a timing diagram. 10

b. List the actions needed to execute the instructions Add R_1, (R_3). Write the sequence of control steps to perform the actions for a single bus structure. Explain the steps. 10

10 a. Explain the 4 stage instruction pipeline with an example. 10

b. In detail, explain hardwired control. 10

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