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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. - Information Science and Engineering

Semester End Examination; Dec. - 2015

Digital Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each **unit**.*

UNIT - I

1 a. Write and explain duality theorem. Simplify $Y = \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + A\overline{B}\overline{C} + AB\overline{C}$, using Boolean laws. 4

b. Simplify the following expression using K - map $f(w,x,y,z) = \Sigma m(0,1,3,7,11,15) + d(2,5)$ and write the circuit diagram for simplified expression. 8

c. Simplify using Quine - McClusky Method : 8

$f(A,B,C,D) = \Sigma m(4,5,6,8,9,10,13) + \Sigma d(0,7,15)$.

2 a. Explain the steps involved in NOR - Gate realization of Boolean expressions.

Realize the expression $f(w,x,y,z) = \overline{w}z + w\overline{z}(x + \overline{y})$ using only NOR - gates. 4

b. Write the simplified POS expression using K - map, 8

$Y = \pi M(0,3,4,7,8,10,12,14) + d(2,6)$

c. Simplify the given SOP expression using Quine - McClusky method, 8

$f(a,b,c,d) = \Sigma m(0,2,3,6,7,8,10,12,13)$

UNIT - II

3 a. Explain the working of Carry look ahead adder and magnitude comparator. 6

b. Realize the function $f(x,y,z) = \Sigma m(0,2,3,5)$ using 4:1 line multiplexer. 6

c. What are parity generators and checkers? With the circuit diagram explain them. 8

4 a. Explain parallel binary adder/subtractor circuit. 6

b. Realize the functions $f_1(X_2,X_1,X_0) = \pi M(0,3,5)$ *and* $f_2(X_2,X_1,X_0) = \pi M(2,3,4)$ using 3-to-8 line decoder and 2 gates. 6

c. What are multiplexer and de-multiplexers? 8

Implement $f(a,b,c,d) = \Sigma m(0,1,2,4,6,9,12,14)$ using 4:1 multiplexer.

UNIT - III

5 a. What are programmable logic devices? With the diagrams explain the working of programmable ROMs. 10

Contd… 2

b. Write the circuit of 4-bit D/A converter and explain the same. 6

c. Write a VDHL code for full adder. 4

6. a. What are programmable array logic devices with the circuit diagram explain a four input and 3-output PAL device. 10

b. What are binary ladders? Where are these used? Explain a binary ladder with a digital input of 100. 10

UNIT - IV

7 a. What is Master-slave flip flop? With the timing diagram, explain how it works. 6

b. Illustrate how JK flip flops can be converted to SR flip flops. 6

c. With circuit diagram explain serial in, serial out and parallel in serial out shifts registers. 8

8 a. Write characteristic equations, truth table, excitation table, state diagram and symbolic diagram of JK flip flop and SR flip flop. 10

b. Differentiate between Ring counter and Johnson ring counter with the circuit diagrams, truth tables and timing diagrams. 10

UNIT - V

9 a. Design an Asynchronous up down counter. 10

b. With circuit diagram and truth table explain a decade counter. 10

10 a. Design a Mod - 6 synchronous counter. 8

b. Differentiate between Mealy and Moore model. Using Moore model give design equations and circuit diagram for sequence detector, where the given sequence is '011'. 12

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