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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. - Information Science and Engineering

Semester End Examination; Dec. - 2015

Digital Design

Time: 3 hrs *Max. Marks: 100*

Note**: Answer any **FIVE** full questions, selecting **ONE** full question from each **unit.

UNIT - I

1 a. Simplify the function $F(A,B,C,D)=\Sigma(0,1,2,5,7,8,9,10,13,15)$ using Quine-Mcluskey method. 10

b. Implement the function $Y=\overline{A}\overline{B}+AB$ using only NAND gates. 5

c. Give the simplest logic circuit for the following logic equation where *d* represent don't care condition: 5

$f(A,B,C,D)=\Sigma m(7)+d(10,11,12,13,14,15)$

2 a. Simplify the given function $f(A,B,C,D,)=\pi(3,4,5,6,11,12)$ for, 5

i) SOP ii) POS

b. Suppose a truth table has a low output for the first three input conditions; 000, 001 and 010. If all other outputs are high, what are the product-of-sums circuits? 5

c. A digital system has 4-bit input from 0000 to 1111. Design a logic circuit that produces a high output whenever the equivalent decimal input is greater than 13. 10

UNIT - II

3 a. Discuss the implementation of a full-adder with two half-adders and an OR gate. 8

b. Explain in detail the process of code conversion from BCD to excess -3 with suitable truth table, maps and circuit diagram. 12

4 a. Briefly explain the 4-bit magnitude comparator with suitable equations and circuit diagrams. 10

b. Realize the functions $f(x,y,z)=\Sigma m(1,3,5,6)$ using 4:1 multiplexer. 6

c. Write a short note on octal-to-binary encoder. 4

UNIT - III

5 a. For a 5-bit resistive divider, determine the following:

(i) The weight assigned to the LSB

(ii) The weight assigned to the second and third LSB

(iii) The change in output voltage due to a change in the LSB, the second LSB, and the third LSB. 8

(iv) The output voltage for a digital input of 10101

Assume 0 = 0 V, and 1 = +10 V.

Contd… 2

b. Explain in detail the concept of D/A converters. Draw a neat sketch of a 4-bit D/A converter and unity gain amplifier. 12

6. a. Discuss the general structure of PLDs with suitable sketch. List the various types of PLDs. 8

b. Explain in detail the two categories of memory with a suitable flow chart for each category. 12

UNIT - IV

7 a. Differentiate between SR flip-flop and JK flip-flop with a suitable logic diagram, truth table for each. 10

b. Define shift register. Explain a 4-bit serial-in-serial out shift register giving its wave forms, circuit diagram and truth table. 10

8 a. Briefly discuss the flip-flop excitation tables of the following flip-flops:

(i) RS (ii) JK

(iii) D (iv) T 8

b. Write short notes on:

(i) BCD Ripple counter

(ii) Johnson counter 12

UNIT - V

9 a. Design a mod-8 synchronous counter using JK flip-flop. 10

b. Differentiate between Moore model and Mealy model with appropriate state transition diagrams. 10

10 a. Explain with a neat logic diagram the concept of a 4-bit up-down binary counter. 10

b. Design a counter with the following binary sequence: 0, 1, 3, 7, 6, 4 and repeat. Use T flip-flops. 10

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