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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. - Information Science and Engineering

Semester End Examination; Dec. - 2015

Computer Organization

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each **unit**.*

UNIT - I

1 a. List the steps needed to execute the machine instruction – Add R_1, R_2, R_3. 6

b. With a diagram, explain the connections between the processor and memory. 6

c. Explain the basic performance equation of a computer. Further indicate different ways to increase the performance. 4

d. Show the little-endian and big-endian representation of multi byte data – 26AC4B17 h, starting from memory address 6000 h. 4

2 a. With a suitable diagram, explain basic input/output operations. 8

b. Explain any six data addressing modes with suitable example. 6

c. Represent the decimal (-10) and 51, as a signed 7 bit number in the following binary formats :
(i) sign –and-magnitude (ii) 1's complement (iii) 2's complement 3

d. Convert the following pairs of decimal numbers to 5 bit, signed, 2's complement binary numbers and add them. State whether or not overflow occurs in each case : 3
(i) -14 and 11 (ii) 7 and 13

UNIT - II

3 a. Describe two methods to handle interrupt requests from multiple devices. 8

b. Explain the distributed arbitration scheme. 8

c. With a neat diagram, explain I/O interface for an input device. 4

4 a. List down the steps carried out during a disk read operation on a SCSI bus. 8

b. With a diagram, explain the input operation on a synchronous bus. 8

c. Define DMA. Explain the registers involved in a DMA operation. 4

UNIT - III

5 a. Give three differences between static RAM and dynamic RAM. Explain the role of memory controller with a diagram. 8

b. Explain the organization of 1K x 1b memory chip. 6

c. Write brief description of : 6
(i) Double-data-rate SDRAM (ii) Latency and bandwidth (iii) EEPROM

Contd… 2

6. a.	Mention one advantage and one drawback of associative cache mapping. Explain direct mapped Cache in detail.	8
b.	Explain two methods of memory interleaving.	8
c.	A block-set-associative cache consists of a total of 64 blocks divided into 4-block sets. Consisting of 128 words, (i) How many bits are there in memory address? (ii) How many bits are there in each of the TAG, SET and WORD fields?	4

UNIT - IV

7 a.	Explain the working of 16 bit carry lookahead adder built using 4 bit adders. Mention the time required to perform 16 bit addition.	10
b.	Compute the product of 010111 x 110110 assuming numbers to be signed 2's complement using both Booth's and Bit-pair coding methods.	8
c.	Mention the best case and worst case multiplier for Booth's multiplication method.	2
8 a.	Show all the steps while performing 1000÷11, using non restoring-division method.	6
b.	What is the need for floating point representation? Explain IEEE single –precision format in detail	8
c.	List the steps to be carried out to perform addition and multiplication of 2 floating point numbers.	6

UNIT - V

9 a.	Draw the diagram to show input and output gating for registers. Further explain : (i) Register transfer (ii) Performing arithmetic or logic operation.	7
b.	With a diagram explain 3-buses organization.	8
c.	Explain hard wired control unit, along with a circuit to generate a control signal.	5
10 a.	Justify the statement "pipeline increases throughput" using a 4-stages pipeline.	10
b.	Briefly explain three possible ways of connecting processors in a multi-processor system.	10

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