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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. - Information Science and Engineering

Make-up Examination; Jan/Feb - 2017

Computer Organization

Time: 3 hrs

Max. Marks: 100

Note: Answer **FIVE** full questions, selecting **ONE** full question from each unit.

UNIT - I

- 1 a. With a block diagram, explain how the memory and the processor are connected? 10
- b. Define the following terms :
- i) Processor clock 6
- ii) Basic performance equation.
- c. List the steps needed to execute the machine instruction Add LOCA, R₀. 4
- 2 a. Define addressing modes. Explain indirect and index addressing modes with example. 8
- b. With the help of a program, explain the function of conditional branch instruction. 6
- c. Represent the decimal values 5, -2 and -10 in the following binary format :
- i) Sign and Magnitude 6
- ii) 1's complement
- iii) 2's complement.

UNIT - II

- 3 a. Describe the three possibilities of enabling and disabling interrupts. 6
- b. Explain the daisy chain method to handle interrupt request from multiple devices. 6
- c. With a diagram, explain centralized arbitration scheme. 8
- 4 a. Explain the input transfer on a synchronous bus using timing diagram. 10
- b. Explain a general 8-bit parallel interface circuit. 10

UNIT - III

- 5 a. Explain how static RAM cells are implemented with a circuit diagram. 6
- b. Describe the internal organization of a 2M x 8 DRAM chip. 10
- c. Define the following :
- i) Memory Access Time 4
- ii) Memory Cycle Time.
- 6 a. Explain PROM and EPROM. 6
- b. Explain the direct mapping cache technique. 6
- c. With a diagram, describe the method of translating virtual memory address into physical address in main memory. 8

UNIT - IV

- 7 a. Design and explain a 4-bit carry-look ahead adder. 6
- b. Write the Booth multiplier recording table and perform $13x-06$ using Booth algorithm. 6
- c. List the steps followed in restoring division algorithm and compute $11001 \div 100$ using the same. 8
- 8 a. Explain single precision and double precision floating point formats. 8
- b. Describe the hardware implementation of floating point addition-subtraction unit. 12

UNIT - V

- 9 a. Explain the process of fetching a word from memory with an example. 10
- b. List the actions and control sequence required for execution of the instruction Add (R3), R1. 10
- 10 a. Describe the hardware control unit organization with block diagram. 8
- b. Show the three possible ways of implementing a multiprocessor system with block diagram. 12

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