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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. - Information Science and Engineering

Semester End Examination; Dec - 2016/Jan - 2017

Computer Organization

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a.	Explain different units of a digital computer with a neat diagram.	8
b.	Define bus. Explain them with their control signals.	7
c.	Explain the different parameters used to evaluate the performance of the computer, providing the basic equation used to compute the performance of the system.	5
2 a.	What is an addressing mode? Explain any four addressing modes with an example.	8
b.	Explain with an example, usage of stacks in a nested subroutine calls.	7
c.	Give reasons to justify using single address, double address and three address instruction to perform the following instruction execution, data at Mem A + data at Mem B $\rightarrow$ Mem C.	5

UNIT - II

3 a.	Explain how interrupt request from several I/O devices can be communicated to a processor through a single INTR Line with a neat configuration diagram and circuit diagram?	10
b.	Explain the hardware registers that are required in a DMA controller chip. Why is it necessary for a DMA controller to be able to interrupt the processor?	10
4 a.	Draw and explain the timing diagram for modified synchronous input data transfer with multiple clock cycles.	6
b.	Explain any two methods of handling multiple I/O devices using interrupts.	7
c.	Explain the general features of interfacing a parallel I/O port to a processor. Explain for key board interface.	7

UNIT - III

5 a.	With a neat circuit diagram, explain RAM and ROM memory cell.	6
b.	Explain any two cache mapping functions.	8
c.	What are the key factors that affect the performance and cost of a computer with respect to memory? Explain briefly.	6
6 a.	Explain the concept of address translation in virtual memory with a neat diagram.	10
b.	Explain asynchronous RAM with a diagram.	7
c.	Write a note on memory hierarchy.	3

Contd.....2

UNIT - IV

7	a.	Give Booth's algorithm to multiply two binary numbers. Explain the working of algorithm taking an example for the following 14 x -5.	12
	b.	Explain the IEEE standards for floating point number.	8
8	a.	Write a neat circuit arrangement for integer division and explain the same.	10
	b.	Work out the multilevel look-ahead carry scheme for doing a 32 bit number addition. How many gate delays are required to do the complete addition in this method?	10

UNIT - V

9	a.	Explain the basic concept of micro programmed control with an neat diagram.	10
	b.	Show the basic organization of a CPU in terms of registers and other units for a single bus data path CPU. In such a CPU, show the complete action of the CPU in fetching and executing the instructions.	10
10	a.	Show the control sequences for execution of Add (R_3), R_1 and explain.	8
	b.	Write the differences between micro programmed versus hardwired control with respect to different attributes.	8
	c.	Mention the different phases involved in the complete execution of an instruction.	4

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