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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

First Semester - Master of Computer Applications (MCA)

Semester End Examination; Jan/Feb. - 2016

Fundamentals of Computer Organization

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each **unit**.*

UNIT - I

1 a. Perform the following number conversions :

(i) $(365)_8 = (\ ?\ )_{16}$

(ii) $(3FD)_{16} = (?\ )_2$ 8

(iii) $(526.72)_{10} = (?)_8$

(iv) $(11011011.100101)_2 = (?)_{16}$

b. Perform the subtraction using 2's complement method :

(i) $(11010)_2 - (10010)_2$ (ii) $(10101100)_2 - (10010011)_2$ 4

c. Express the following function in a sum of min terms and product of max terms :

(i) $F(a, b, c, d) = a'c' + bd$ (ii) $F(A, B, C) = (A' + B')(B' + C)$ 8

2 a. Perform the BCD addition of 184+576 results should be in BCD. 4

b. Find the complement of the function F(A, B, C) = A+BC in canonical form and write the truth table. 5

c. 62-23 using 2's complement and 9's complement. 5

d. Explain Huntington's Postulates. 6

UNIT - II

3 a. Simplify using K-map method,

$F(A, B, C , D) = \Sigma(0, 3, 4, 5, 7) + d(8, 9, 10, 11, 12, 13, 14, 15)$ 6

b. Design a full adder with truth table and logic circuit using only NAND gates. 8

c. What are universal gates? Why they are called so? Construct X-OR and X-NOR using only OR gate. 6

4 a. Simplify the Boolean function $F(A, B, C, D) = \Sigma(0, 1, 2, 5, 8, 9, 10)$ in SOP and POS construct the circuit for both the simplified function. 8

b. 'NOR is Universal gate' support with the necessary diagrams and explanation. 6

c. What is multiplexer? Design 4-1 line multiplexer. 6

UNIT - III

5 a. Construct and explain the working of a 3 to 8 decoder. 10

Contd…..2

b. With a neat diagram explain how the instruction Add R_0, R_1 is executed in the computer. 10

6 a. What is Bus? Explain Single bus structure. 4

b. Explain different functional units of digital computer with neat diagram. 10

c. Explain the working of 3-bit down Ripple counter. 6

UNIT - IV

7 a. How interrupt requests from several I/O devices can be communicated to a processor through a single INTR line? Explain how multiple interrupts can be handled. 10

b. Write a program that can evaluate the expression Z = A*B + C*D using one address, two address and three address instruction formats. 10

8 a. What is bus arbitration? Explain two approaches to bus arbitration. 10

b. What is an addressing mode? Discuss any 4 addressing modes. 10

UNIT - V

9 a. What is DRAM? With neat diagram explain internal organization of asynchronous 2M x 8 dynamic memory chip. 10

b. Define virtual memory. Explain the translation process of memory address from its virtual address into physical address. 10

10 a. What is ROM? Explain the different types of ROM's. 10

b. Define Cache memory. Explain how mapping is performed in set associate memories. 10

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