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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

First Semester, M. Tech - Computer Engineering (MCEN)

Semester End Examination; Jan - 2017

Advanced Computer Architecture

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Explain the different classes of computers. 9

b. What is ISA? Briefly explain the following dimensions of ISA :

i) Classes of ISA ii) Addressing modes 9

iii) Control flow instructions iv) Encoding ISA.

c. Find the number of dies per 300 mm wafer for die that is 1.5 cm on a side. 2

2 a. Explain the following principles of computer design : 6

i) Parallelism ii) Locality Principle iii) Focus on common case.

b. Explain Amdahl's law. Suppose that we want to enhance a processor such that new processor is 20 times faster than the old for an application. Also assume that the original processor is 50% computation bound and 30% IO bound. Find the overall speed up. 5

c. What is dependability? Explain the measures of dependability. 9

UNIT - II

3 a. Define pipelining. Explain the five stage pipeline for a RISC processor. 10

b. Describe the major hurdles of pipelining-pipeline hazards (any two). 10

4 a. Explain the basic pipeline for MIPS. 10

b. Discuss the various methods for dealing with pipeline stalls due to branch delay. 10

UNIT - III

5 a. Explain Dynamic Branch prediction with example (2 bit prediction scheme). 8

b. Explain loop level parallelism. 4

c. Explain the following : 8

i) Data Dependences ii) Data Hazards.

6 a. Explain the basic structure of Tomasulo's based MIPS floating point unit with a diagram. 10

b. Explain Branch-Target Buffer with example. 10

UNIT - IV

7 a. Explain Cache Coherence protocol for Write-Back cache with state diagrams. 10

b. Explain Flynn's model for categorizing all computers. 6

c. Draw a block diagram of centralized shared memory multiprocessor. 4

Contd…2

8 a. Explain snooping protocols. 8

b. Explain different models of memory consistency. 12

UNIT - V

9 a. Discuss the following advanced cache optimization techniques :

i) Small and simple caches

ii)Prediction

iii) Trace caches

iv) Pipelined caches

v) Non blocking caches. 10

b. Explain any five basic cache optimization techniques. 10

10 a. How processes are predicted using virtual memory and virtual machines. 12

b. Explain Internal organization of 64-bit DRAM. 8

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