



P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

First Semester, M. Tech - Computer Engineering (MCEN)

Semester End Examination; Jan/Feb. - 2016

Advanced Computer Architecture

Time: 3 hrs

Max. Marks: 100

Note: Answer FIVE full questions, Selecting ONE full question from each unit.

UNIT - I

- 1 a. Some microprocessors tooling are designed to work adjustable voltage, so that 15% reduction in voltage may result in 15% reduction in frequency. What would be the impact on dynamic power? 4
- b. Which are the implementation technologies that are critical to modern implementations? 8
Explain the performance trends: Bandwidth over latency.
- c. Explain the quantitative principles of computer design. 8
- 2 a. Explain the different classes of computer. 8
- b. Summarize the trends in technology, cost and power in development of computers. 8
- c. What is dependability? Explain the measures of dependability. 4

UNIT - II

- 3 a. Explain the five stage pipeline for a RISC processor. 12
- b. Explain what makes pipelining hard to implement. 8
- 4 a. Explain the MIPS pipeline is extended to handle multicycle operations and floating point operations. 10
- b. Explain the major hurdles of pipelining-pipeline Hazards. 10

UNIT - III

- 5 a. What is dynamic scheduling? Explain Tomasulo's algorithm. Give example. 10
- b. With a neat diagram explain the basic structure of FP unit using Tomasulo's algorithm; extended to handle speculation. 10
- 6 a. With a neat diagram explain the Pentium 4 micro architecture. Give an analysis of performance of Pentium 4. 12
- b. How many bits are in the (0, 2) branch predictor with 4k entries? How many entries are in a (2, 2) predictor with the same number of bits? 4
- c. Explain loop unrolling. 4

UNIT - IV

- 7 a. Explain the implementation of directory based cache coherence protocol. 10
- b. Explain the sum T1 multiprocessor architecture. 10

- 8 a. Assume that L2 has a block size four times that of L1. Show how a miss for an address that causes a replacement in L1 and L2 can level 1 to violation of the inclusion property. 4
- b. What is synchronization? Explain how locks are implemented using coherence. 8
- c. Explain model of memory consistency. 8

UNIT - V

- 9 a. Explain the different memory technologies. Explain how memory performance can be improved. 10
- b. What are advanced optimizations of Cache Coherence? Explain any five optimizations of Cache Coherence 10
- 10 a. Explain protection Via virtual memory and virtual machine. 10
- b. Explain the issues in the design of memory hierarchies. Explain how this is implemented in AMD operations. 10

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