***U.S.N*** | | | | | | | | | | |

# P.E.S. College of Engineering, Mandya - 571 401

***(An Autonomous Institution affiliated to VTU, Belgaum)***

**First Semester, M. Tech – VLSI Design and Embedded System (MECE)**

**Semester End Examination; Jan - 2017**

**CMOS VLSI Design**

*Time: 3 hrs* *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

## UNIT - I

1 a. Analyze the second order effect on IC performance with respect to, i) Sub threshold conduction ii) Tunneling iii) Punch through effect. 6

b. With VTC, explain the impact of variations in β values by considering CMOS inverter. 6

c. Explain the working of differential inverter with circuit diagram and transfer characteristics. 8

2 a. Obtain the small signal equivalent of MOSFET and the corresponding expression for *g*. 8

b. Derive an expression for $NM_L$ and $NM_H$. 7

c. Realize the schematic of tristate inverter and BiCMOS inverter. 5

## UNIT - II

3 a. Explain the steps of fabrication process of NMOS technology. 9

b. Show that the delay time and transit time are interchangeable [consider sum technology]. 6

c. Realize the CMOS schematic and the corresponding stick diagram of $NOR_3$ gate. 5

4 a. Obtain the scaling factors for the following parameters ; i) Operating frequency ii) Power dissipation iii) Switching energy. 6

b. Derive an expression for delay in driving a large capacitance load in a chain of inverters with varying sizes. 8

c. Realize the symbolic diagram of $NAND_2$ gate and $NOR_2$. 6

## UNIT - III

5 a. Realize the function using transmission gates (TG), i) $F = \overline{A} + AB + A\hat{B}C$ ii) $F = A\overline{B} + \overline{A}BC + AB\overline{C}$. 6

b. Discuss the cascading problem in Dynamic logic circuit using schematic and waveform. 6

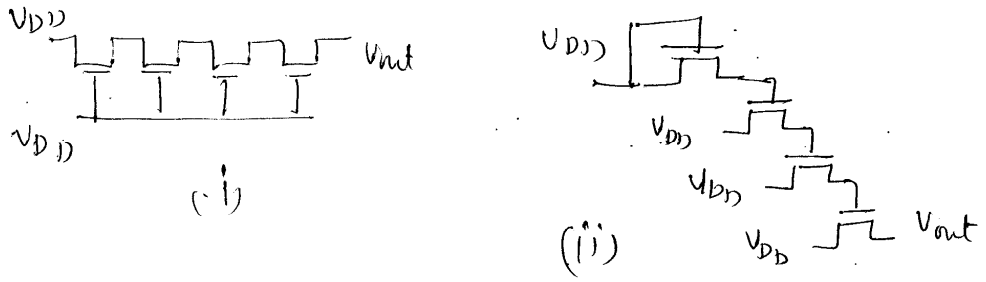
c. Explain the boot strapping principle and derive an expression for $C_{boot}$. 8

6 a. Obtain the Euler path for the function $F = \overline{A(D+E)+BC}$. 6

b. With gate level, CMOS schematic and waveform, explain SR latch (NOR based). 10

c. Find the output voltage for the following arrangements. Given $V_{DD}$ = 3.8 V, $V_{Tn}$ = 0.7 V. 4

Contd…2



**UNIT - IV**

7 a. With necessary diagram and expression, explain the working of differential amplifier. 10

b. Derive an expression for $V_{REF}$ using Band gap reference concept. 10

8 a. Explain the concept of current mirrors along with an example. 10

b. Explain the principle of band gap reference. Write the expression for $V_{REF.}$ 10

**UNIT - V**

9 a. List the causes and remedies for latch-up in CMOS inverter. 10

b. Explain the charge sharing phenomenon with an example. 6

c. Briefly discuss the H-tree and Buffered clock distribution network. 4

10 a. Explain latch up in CMOS inverter with necessary diagrams. 8

b. With a neat diagram, explain Domino logic concept. 6

c. Discuss any three clock generating technique. 6

* * *