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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

First Semester, M. Tech - VLSI Design and Embedded System (MECE)

Make-up Examination; Feb - 2017

CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Discuss the working of nMOS enhancement mode transistor in different regions of operation with neat sketches and output characteristics. 10

b. Explain the DC characteristics of the CMOS inverter with different regions of operation. 10

2 a. List the second order effects in a MOSFET. Briefly explain. 12

b. Explain the pseudo nMOS inverter and differential inverter. 8

UNIT - II

3 a. Discuss the Lambda based design rules as applicable to MOS layers and transistors. 10

b. Show that the expressions for rise time delay and fall time delay of a CMOS inverter is $t_f = 4\frac{C_L}{\beta_h V_{DD}}$ and $t_r = 4\frac{C_L}{\beta_p V_{DD}}$. 10

4 a. Sketch the fabrication process of a CMOS inverter and briefly discuss the each step. 12

b. Draw the CMOS circuit diagram, stick diagram and layout of a two input NAND and NOR gate. 8

UNIT - III

5 a. Discuss the working of CMOS transmission gate. Describe the different regions of operations and associated equations. 10

b. Draw the gate level symbol and CMOS NOR based SR Latch and explain the operation and transient analysis of SR latch. 10

6 a. What is pass transistor? Describe how logic '0' transfer and logic '1' transfer takes place in pass transistor. 10

b. Explain the operation of voltage bootstrapping with suitable circuits and equation. 10

UNIT - IV

7 a. Explain the differential amplifier with a neat circuit diagram. 10

b. Discuss the different types of current mirror circuits. How can these be used in the design of a differential amplifier. 10

8 a. Explain the cross operations amplifier with necessary expression and characteristics. 10

b. Analyze the performance of band gap reference due to variation in temperature. 10

Contd…2

UNIT - V

9	a.	List the advantages and disadvantages of CMOS over nMOS technology.	10
	b.	What is the latch V_p in bulk CMOS? Mention the causes and prevention of latch up problem in CMOS inverter.	10
10	a.	Explain the clock generation and clock distribution type and storages types in dynamic CMOS inverter circuits.	10
	b.	Differentiate between CMOS and Silicon-On-Insulator (SOI) Technology.	5
	c.	Differentiate between nMOS and CMOS fabrication process.	5

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