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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

First Semester, M. Tech – VLSI Design and Embedded System (MECE)

Make-up Examination; July - 2016

CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Analyze the body effect in nMOS structure. 6

b. Obtain the expression for g_{ds} and g_m in linear and in saturation region. 8

c. Define noise margin. Obtain the expression for low and high noise margin. 6

2 a. Discuss the second order effects in MOSFET with respect to,
i) Mobility variation ii) Drain punch through. 8

b. Analyze the performance of CMOS inverter with respect to variation in β. 8

c. Obtain the schematic of inverter using,
i) CMOS ii) BiCMOS iii) Transmission gate. 4

UNIT - II

3 a. Obtain the scaling factor for the following parameters,
i) Channel resistance ii) Max. operating frequency iii) Power – speed product. 8

b. Determine sheet resistance for,
i) NMOS inverter ii) CMOS inverter. 6

c. Derive an expression for propagation delay in a chain of inverter stages. 6

4 a. With neat fabrication structure, explain the n-well CMOS process. 10

b. Derive an expression for rise time and fall time by considering CMOS inverter. 10

UNIT - III

5 a. Obtain the capacitance schematic of CMOS NAND2. 6

b. Bring out the differences between AOI and OAI logic. 8

c. Realize the schematic of CPL,
(i) NAND / AND (ii) NOR / OR. 6

6 a. Define Euler path. Explain with an example. 8

b. Derive an expression for C_{boot} using boot strapping principles. 6

c. Analyze the performance of dynamic logic circuits. 6

Contd…2

UNIT - IV

7	a.	Analyze the performance of Differential amplifier with relevant diagram and expression.	10
	b.	Derive an expression for V_{ref} in band gap reference.	10
8	a.	Derive an expression for A_v in differential amplifier along with small signal equivalent circuit.	10
	b.	Analyze the performance of band gap reference due to variation in temperature.	10

UNIT - V

9	a.	Discuss the causes for latch up in n-well CMOS inverter. Mention the remedies for latch-up.	10
	b.	Along with schematic, discuss the working of any three clock generation technique.	10
10	a.	Discuss the charge sharing phenomenon in Domino logic circuit with an example.	10
	b.	Analyze the performance of clock distribution network.	10

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