U.S.N | | | | | | | | | | |

P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

First Semester, M. Tech - Electronics and Communication Engineering

(VLSI Design and Embedded Systems)

Semester End Examination; Jan/Feb. - 2016

CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each **unit**.*

UNIT - I

1 a. Derive an expression for threshold voltage in terms of built in potential and work function. 8

b. Analyze the impact of variation in β on the transfer characteristics of CMOS inverter. 6

c. With the output characteristic and equivalent circuit. Briefly explain the working of transmission gate. 6

2 a. Obtain the equivalent circuit of CMOS inverter in all five regions of operations. 6

b. With the schematic and transfer characteristics. Explain the working of differential inverter. 8

c. Explain the different approaches in realizing BiCMOS inverter. 6

UNIT - II

3 a. What is the need of design rules of fabrication technology? Mention the two types of design rule. 6

b. Explain 2 phases of diffusion procession in fabrication of VLSI circuits. 8

c. Justify "The delay time and transit time are interchangeable". 6

4 a. Determine the scaling factor for the following design parameters :

(i) Gate delay

(ii) Saturation Current

(iii) Switching energy per gate 6

b. Discuss the alternate ways of realizing gate. 6

c. Derive an expression for total delay in a cascaded pass transistors (Connected in series). 8

UNIT - III

5 a. Draw the schematic of CMOS NOR2 gate with associated parasitic capacitances. What will be the value of V_{th} in terms of V_{DD}? 6

b. Explain the working of AOI based implementation of the closed NOR based SR latch. 8

c. Justify "Dynamic CMOS logic gates driven by same signal cannot be cascaded directly". 6

6 a. Obtain the CMOS schematic and its corresponding Euler path for the function $Y = \overline{BC + A(D + E)}$. 4

Contd…..2

	b.	Discuss the timing limitations of NOR based clocked JK latch circuit along with timing diagram.	8
	c.	Analyze the pipelined architecture of NORA CMOS logic (NP-DOMINO logic).	8

UNIT - IV

7	a.	Explain the working of common source amplifier using MOSFET and derive an expression for gain.	10
	b.	Derive an expression for trans conductance in CMOS differential amplifier with relevant diagrams and waveform.	10
8	a.	Current mirrors are used in the design of CMOS circuits. Why? Explain with necessary schematic.	10
	b.	Starting from fundamentals derive an expression for V_{REF} in terms of V_{GO} and V_{to} with respect to Band gap reference.	10

UNIT - V

9	a.	With cross sectional view, explain latch up in n-well CMOS inverter. Mention the causes for latch up.	12
	b.	Discuss the two important schemes adopted for clock distribution.	8
10	a.	Analyze the charge sharing in CMOS circuit design.	8
	b.	Discuss the different types of clock generation.	12

* * *