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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

First Semester, M. Tech - Electronics and Communication Engineering

(VLSI Design and Embedded Systems)

Make – up Examination; Feb - 2016

CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each **unit**.*

UNIT - I

1 a. Describe the working on n-MOS enhancement mode transistor with diagram and output characteristics. 10

b. Define the body effect in MOSFET. Derive the MOSFET current equation, in different regions operation. 10

2 a. Explain the significance of channel length modulation and hot electron effect in MOS devices. 10

b. Explain the trends in transfer characteristics with β_n/β_p ratio's, using suitable mathematical analysis. 10

UNIT - II

3 a. Explain λ based design rules as applicable to MOS layers and transistors. 10

b. Derive the scaling factors for the following CMOS parameters :

i) Gate Capacitance C_g ii) Power speed product

iii) Number of gates N iv) Parasitic capacitance

v) Channel resistance 10

4 a. Explain twin tub CMOS process. 10

b. Draw the CMOS circuit diagram and the stick diagram for

i) 2 input **NAND** gate ii) 2 input **XOR** gate 10

UNIT - III

5 a. Describe the behaviour of bistable element. Derive the expression for the output voltage. 8

b. Bring out the differences between AND-OR-Inverter (AOI) logic and OR-AND-Inverter (OAI) logic with suitable example. 5

Contd…..2

c. Explain briefly the SR latch with gate level schematic, truth table and CMOS circuit. 7

6 a. What is pass transistor? Describe how does logic '0' transfer and logic '1' transfer takes place in pass transistor. 10

b. Draw the dynamic CMOS logic and explain the pre-charge and evaluation mode. 4

c. Dynamic CMOS logic circuits cannot be cascaded. Why? Explain. 6

UNIT - IV

7 a. Explain the differential amplifier with a neat CMOS circuit and cross section. Obtain the expression for transconductance of differential amplifier. 10

b. Starting from the fundamentals derive an expression for the reference voltage V_{REF} in a conventional CMOS bandgap reference. 10

8 a. Explain the different types of current mirror circuits. How can these be used in the design of a differential amplifier? 10

b. Explain cross operational amplifier with necessary expression and characteristics. 10

UNIT - V

9 a. What is domino CMOS logic? Compare it with conventional CMOS logic. Justify the same with one example each. 10

b. What is latch up in CMOS inverter? Mention the causes for latch up and how is it minimized? 10

10 a. Bring out the differences between n-MOS and CMOS fabrication process. 5

b. Realize the following function Z = (A+B) + (C+D) (E+F) + GH using 5
i) Static CMOS ii) Domino CMOS

c. Explain how clock signal can be generated, distributed, and stored in dynamic CMOS inverter circuits. 10

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