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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Second Semester, M. Tech - VLSI Design and Embedded System (MECE)

Make-up Examination; July - 2016

Design of Analog and Mixed Mode VLSI Circuits

Time: 3 hrs *Max. Marks: 100*

***Note**: i) Answer **FIVE** full questions, selecting **ONE** full question from each unit.*
ii) Assume missing data suitably.

UNIT - I

1 a. Discuss the channel length modulation concept and substrate effect and hence, develop the complete circuit model of MOSFET for small signal operation, considering device capacitances. 8

b. For the CS stage with diode-connected load, shown in Fig. 1. Derive the expression $\frac{\partial V_{out}}{\partial V_{in}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \cdot \frac{1}{1+\eta}$ with usual notations. 4

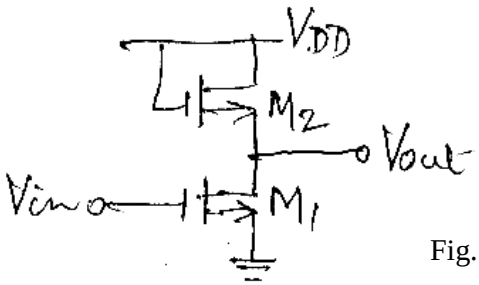

Fig. 1: CS stage with diode-connected load.

c. Prove that $\frac{\partial V_{out}}{\partial V_{in}} = g_m(1+\eta)R_D$ for the circuit shown in Fig.2 and sketch the input-output characteristics. 8

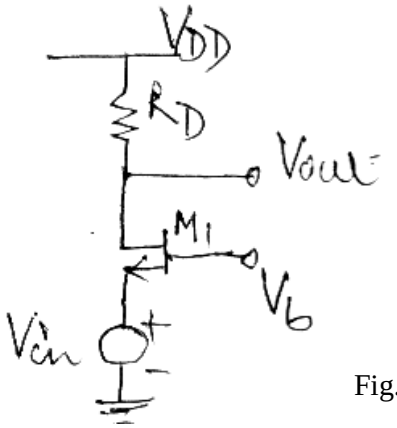

Fig. 2: CG Stage

2 a. Considering the resistance and body effect, derive the expression for the small signal voltage gain and output resistance for source follower circuit with current source. Draw the equivalent circuit. 12

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b. Calculate the input resistance of CG stage shown in Fig. 3 and draw the small-signal equivalent circuit.

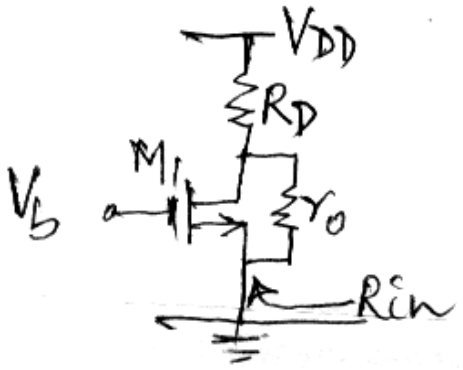

Fig. 3: CG Stage 8

UNIT - II

3 a. For the differential pair shown in Fig. 4, derive an expression for (I_{D1} - I_{D2})

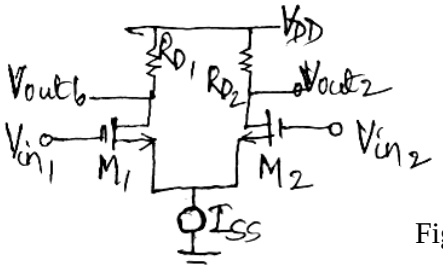

Fig. 4: Differential pair 8

b. Develop the circuit of Gilbert cell starting from the basics of differential pair. 12

4 a. Explain with a circuit diagram, the realization of cascode current mirror using cascode current source. 8

b. Develop the expression for CMRR in a differential pair with active current mirror sensing common mode change. 12

UNIT - III

5 a. Draw the circuit of a source follower with output capacitance and its high frequency equivalent circuit. Derive the expression for the transfer function. 10

b. Draw the source follower circuit showing noise sources and develop the expression for the input referred noise voltage. 10

6 a. For the simplified cascade stage shown in Fig. 5, neglecting the body effect ($\gamma = 0$), calculate the transfer function (V_{out}/ V_{in}). 10

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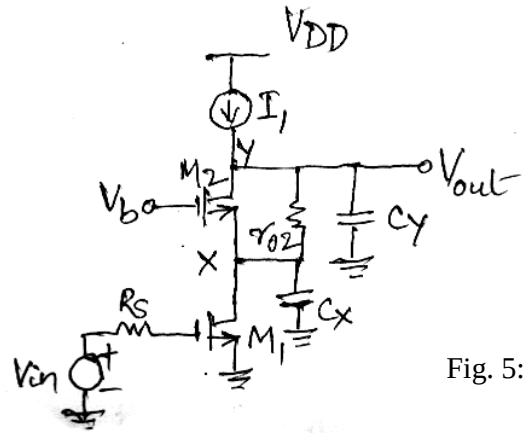

Fig. 5: Simplified cascode stage at high frequencies

b. Draw the differential pair circuit including input-referred noise sources and prove that the input noise squared of differential pair is twice the input noise voltage squared of a common-source state. 10

UNIT - IV

7 a. Draw the circuit implementation of two-stage Op-AMP and explain the functions of each state. 6

b. Discuss the various methods of boosting the gain in differential cascade. 6

c. Discuss the response of a linear Op-AMP to a step input and hence obtain the expression for the output voltage, sketch the circuit diagram and relevant waveforms. 8

8 a. Calculate the expression for the input-referred thermal noise voltage of a two-stage Op-AMP. 10

b. Derive the expression for the low-frequency PSRR of the feedback circuit shown in Fig. 6.

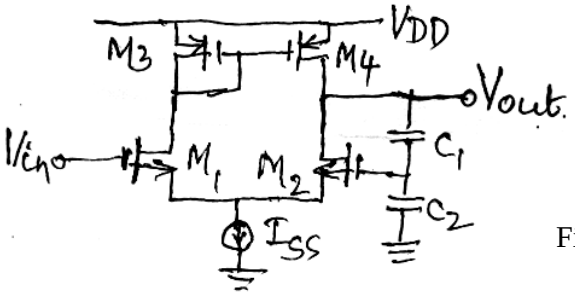

Fig 6: Differential pair with active current mirror and feedback 10

UNIT - V

9 a. Sketch the circuit of three stage ring oscillator and explain the important aspects of closed loop transfer function. 8

b. Draw the cross-coupled oscillator circuit with tail current source and describe how the problems of conventional oscillators are overcome. 12

10 a. Discuss the response of a phase locked loop (PLL) of a phase step and frequency step. 12

b. Explain the problem of lock acquisition and its solution in type-I PLL. 8

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