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P.E.S. College of Engineering, Mandya - 571 401 (An Autonomous Institution affiliated to VTU, Belgaum) Second Semester, M. Tech - Electronics and Communication Engineering (VLSI) Semester End Examination; June - 2016 Design of Analog and Mixed Mode VLSI Circuits Time: 3 hrs Max. Marks: 100				
Ne	ote: Answer FIVE full questions, selecting ONE full question from each unit.			
	UNIT - I			
1 a.	Derive the expression for I_{D} of a MOS transistor starting from the basics and hence obtain the			
	expressions for I_D when the device operates in,	10		
	(i) Triode region	10		
	(ii) Saturation region.			
b.	Discuss the second order effects in a MOS device.	10		
2 a.	Obtain the expression for voltage gain of CS amplifier using small signal analysis for the			
	following loads :			
	(i) Resistive load, R _D	10		
	(ii) Diode connected load			
	(iii) Current source load.			
b.	Obtain the expression for input impedance of CG stage taking channel length modulation and	10		
	body effect into consideration.	10		
UNIT - II				
3 a.	For a basic differential pair, show that under equilibrium,	10		
	$\left A_{v}\right = \sqrt{\mu_{c}C_{ox}\left[W/L\right]I_{SS}R_{D}}$	10		
b.	For an active current mirror processing a signal obtains the expressions for R_{out} and A_v .			
	Explain how the drain currents of M_1 and M_2 are combined?	10		
4 a.	Explain the operation of cascode current mirror and also discuss how gate voltage bias is			
	generated?	10		
b.	Discuss the common mode response of differential pair :			
	(i) In the presence of resistor mismatch	10		
	(ii) With finite tail capacitance.			
	UNIT - III			
5 a.	For a source follower, using its high frequency equivalent circuit, obtain the expression for			

5 a. For a source follower, using its high frequency equivalent circuit, obtain the expression for $V_{out}(s)/v_{in}(s)$ and hence obtain the expression for significant pole. 10

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b.	For a common source stage obtain the expressions for $V_{out}(s)/V_{in}(s)$ and the pole frequencies.	10	
6 a.	Discuss the high frequency response of cascode stage.	10	
b.	For a differential pair, using its high frequency model obtain the expression for $\frac{V_o(s)}{V_i(s)}$.	10	
UNIT - IV			
7 a.	Explain the operation of single stage folded cascode Op-Amp.	10	
b.	What is gain boosting? Explain how gain boosting is done in a differential cascode stage?	10	
8 a.	Discuss the Response of linear Op-Amp to step input.	10	
b.	Discuss the compensation in a two-state Op-Amp.	10	
UNIT - V			
9 a.	For a Colpitts oscillator obtain the expressions for,		
	(i) Frequency of oscillations	10	
	(ii) Min gains for sustained oscillations.		
b.	Develop the linear model of Type-I PLL and discuss its step response.	10	
10 a.	For a unity gain switched capacitor amplifier, obtain the expression for,		
	$\frac{V_{Out}(s)}{V_{in}(s)}$ and hence obtain the expression for its time constant.	10	
b.	Discuss the methods of generating temperature independent reference voltage.	10	

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