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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Second Semester, M. Tech - VLSI Design and Embedded System (MECE)

Make - up Examination; July - 2016

Low Power VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1	a.	Briefly analyze the need for low power in VLSI chips.	8
	b.	By considering dynamic NAND2, derive an expression for energy stored in terms of V_{DD}.	6
	c.	Discuss the principles of low power design.	6
2	a.	Discuss the transistor sizing by considering a chain of inverter stages (N Stages).	6
	b.	Analyze the problems associated with transistor and gate sizing for dynamic power reduction.	4
	c.	Discuss the impact of technology scaling and innovation trends for low power devices.	10

UNIT - II

3	a.	Briefly analyze the gate level analysis based on event driven logic simulation.	6
	b.	Write a note on static state power analysis by considering the different implementation of NAND2 gate.	6
	c.	Discuss the architecture level analysis of power models based on activities.	8
4	a.	Discuss the capacitive power dissipation by considering gate level power analysis based on logic simulation.	4
	b.	Bring out the differences between positive correlation and negative correlation with an example.	6
	c.	Derive an expression for minimum number of samples N required for stopping criterion of simulation using Monte Carlo concept.	10

UNIT - III

5	a.	Analyze the behavior of discrete random signals due to variation in frequency and its static probability.	4
	b.	Given P(a), P(b), and P(c) are input static probabilities. Determine output probability of y = ab + c using Shannon's decomposition method.	6
	c.	Discuss the power estimates using entropy and derive an expression for the same.	10
6	a.	Explain the working of single edge triggered and double edge triggered flip flops along with schematics.	10
	b.	Obtain the logic diagram for 3 input functions under the NPN equivalence relation (Any 5).	10

Contd…2

UNIT - IV

7	a.	Explain the architecture of bus invert encoding along with diagram of relevant expressions.	10
	b.	Analyse the precomputation architecture based on Shannon's decompositions. Hence explain latch based pre computation architecture.	10
8	a.	Bring out the differences between parallel processing and pipelined systems along with block diagram.	10
	b.	Analyze the flow graph transformation with operator reduction.	10

UNIT - V

9	a.	Bring out the differences between single drivers versus distributed buffers.	10
	b.	Analyze the power dissipation in clock distribution networks.	10
10	a.	Explain the algorithmic load analysis and optimization.	10
	b.	Discuss the performance variations by considering architectural level estimation and synthesis of power.	10

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