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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Second Semester, M. Tech - VLSI Design and Embedded System (MECE)

Make-up Examination; Jan/Feb - 2017

Low Power VLSI Design

Time: 3 hrs *Max. Marks: 100*

Note: *Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. For a long channel n-MOSFET, derive the expression for sub threshold current. Also explain the short channel effect. 10

b. With usual notation, derive the expression for the short circuit power dissipation in a CMOS inverter. 10

2 a. Discuss the impact of transistor sizing, gate oxide thickness and technology scaling on low power electronics with suitable diagram. 10

b. Derive an expression for depth of depletion region and charge in the inversion layer by considering MIS structure. 10

UNIT - II

3 a. With a neat diagram, explain the dual bit type signal model for DSP system. Explain how data path module is characterized for the module, with one input and one output such as a FIFO queue, with relevant capacitance and power expression? 10

b. Discuss in brief about spice basics, spice power analysis. Also explain the discrete transistor modeling and analysis 10

4 a. Briefly explain entropy and explain in detail how power estimation is done using entropy analysis of combinational circuit? 10

b. What is the significance of Monte Carle simulation? Explain clearly all the terms associated in estimation of number of simulation sampler. 10

UNIT - III

5 a. Discuss the expected frequency and static probability of discrete random signals. 6

b. Analyze the propagation of static probability in logic circuit with an example. 6

c. Along with block diagram and schematic, explain the working of single edge triggered flip flop. 8

6 a. Derive an expression for conditional probability and frequency by considering signal model. 6

b. Estimate the power in combinational logic using entropy analysis. 6

c. Along with block diagram and schematic explain the working of double edge triggered flip flop. 8

Contd….2

UNIT - IV

7	a.	What is meant by gate reorganization? Explain the various local transformation operators for gate reorganization.	8
	b.	Name the different techniques used for switching activity reduction in CMOS circuit. Briefly explain any one.	6
	c.	Explain the pre-computation logic in binary comparator function block.	6
8	a.	With the help of transition analysis, explain the mapping of control flow graph to hardware architecture.	6
	b.	What is pre-computation logic? Explain typical pre-computation architecture.	6
	c.	What do you mean by power management? With a neat block diagram, explain adaptive performance management by voltage control.	8

UNIT - V

9	a.	Bring out the differences between single driver and distributed buffers.	8
	b.	Explain with relevant information on algorithmic level analysis and optimization.	12
10	a.	Bring out the differences between zero skew and tolerable skew.	8
	b.	Explain the necessary information on architectural level estimation and syntheses.	12

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