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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

First Semester, M. Tech. – Electronics and Communication Engineering

(VLSI Design and Embedded Systems)

Semester End Examination; Jan/Feb - 2016

Digital System Design using Verilog

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each **unit**.*

UNIT - I

1 a. Explain the design method for hardware /software co-design with neat design flow diagram. 10

b. Suppose, for a family of logic components, V_{IL} is 0.6 V and V_{IH} is 1.2 V. What voltages are required for V_{OL} and V_{OH} to provide a noise margin of 0.2 V? 4

c. Suppose a factory has a vat with a sensor that outputs '1' when the vat is empty, a '0' otherwise. The vat also has a pump to empty it, and a control switch to activate the pump. Device a circuit that turns the pump on when the switch is set to activate the pump and the vat is not empty. 6

2 a. Design an encoder using Verilog HDL for use in a domestic burglar alarm that has sensor for each of eight zones. Each sensor that is '1' when an intrusion is detected in that zone and '0' otherwise. The encoder has three of output; encoding the zone as followed,
Zone1: 000, Zone 2: 001 …… Zone 8 : 111. 10

b. Write Boolean equations for a BCD decoder, that is a decoder that has a BCD code word as input and that has outputs y_0 through y_9. Draw a circuit that uses AND and OR gates and inverters to implement the decoder. 6

c. Use a 2 - to - 1 multiplexer to implement a circuit whose output is given by the Boolean expression a.(b + $\overline{c}$) when enable.$\overline{sel}$ is '1', and the Boolean expression $x \oplus y$ otherwise. 4

UNIT - II

3 a. Develop a Verilog model of a converter that connects from a 4 - bit designed binary code input to a 4 - bit Gray coded output. 6

b. Show how a 2's complement adder / subtractor can be used to compute the absolute value of number. Hint : $y = 0 + y$ and $-y = 0 - y$. 6

c. Develop a 3 - bit shift register implemented with D - flip-flops and multiplexer. 8

4 a. Write a Verilog model for a complex multiplier data path showing data path for a sequenced complex multiplier. 10

b. Obtain the state diagram for a serial adder as a Moore sequential network. 10

Contd...2

UNIT - III

5	a.	Explain the difference between synchronous and asynchronous static RAM using timing diagram.	10
	b.	Explain multi - point memories. Develop a Verilog model of a dual point 4k x 16 bit flow through synchronous RAM. One point allowed data to be written and read while the other point only allowed data to be read.	10
6	a.	Compute 12 - bit ECC word corresponding to the 8 - bit data word 10110101.	4
	b.	Explain the PROM logic with example.	10
	c.	Describe differential signaling. How does it improve noise immunity?	6

UNIT - IV

7	a.	Describe the instruction encoding of the Gumnet processor.	10
	b.	Describe the organization of an embedded digital system. How it is modified for higher performance?	10
8	a.	Explain Flash ADC and successive approximation ADC with neat diagram.	12
	b.	Explain R/2R ladder DAC with neat diagram.	8

UNIT - V

9	a.	Develop a Verilog model for the Sobel accelerator bus slave interface.	10
	b.	Discuss built - in - self - test technique with an example of a circuit that generates test pattern (vectors).	10
10	a.	Explain a 4 - bit LFSR for generating pseudo - random test vector and write a Verilog code for the same.	12
	b.	Discuss various design optimization techniques.	8

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