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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

First Semester, M. Tech – VLSI Design and Embedded System (MECE)

Semester End Examination; Jan - 2017

ASIC Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Explain full custom ASIC. List the advantages and disadvantages of full custom ASIC. 6

b. Discuss the different choices of ASIC Cell libraries. 6

c. Explain the ASIC design flow. 8

2 a. Explain the types of gate array based ASICs. 10

b. Explain the essential characteristics of an FPGA. 6

c. Write a note on standard cell based ASICS. 4

UNIT - II

3 a. Encode the binary number,

i) b = 011 as a CSD vector

ii) b = 101001 as a radix - 4 vector. 6

b. Explain carry save addition with its advantages. 8

c. Explain the conditional sum adder. 6

4 a. Show that optimum delay is given by,

$D = NF^{1/N} + P + Q$. 6

b. Define logical effort and electrical effort. 4

c. Compute the delay involved in implementing the following function as a multistage AOI logic,

$IN(A_1, A_2, B_1, B_2, C) = NOT (NAND (NAND (A_1, A_2) AOI 21 (B_1, B_2, C)))$. 10

UNIT - III

5 a. Draw and explain the flat schematic for a 4-bit D Latch and its vectored instance cell with a cordinality of four. 10

b. What is need for hierarchical design? With suitable example, explain the hierarchical design. Also explain how to label the nets in the hierarchical design. 10

6 a. What is net list screener? Mention the errors that can be found by it and explain them. 10

b. Explain schematic entry for ASICs. 6

c. What you mean by Back-Annotation? 4

Contd…2

UNIT - IV

7	a.	Explain Shannon's expansion theorem.	6
	b.	Explain ACTEL ACTI logic module as a Boolean function generator.	8
	c.	Compare ACTEL ACTI with Xilinx XC 3000.	6
8	a.	Explain the different types of I/O requirements used in programmable ASIC.	6
	b.	With the help of block diagram, explain Xilinx XC 4000 IOB.	8
	c.	Explain the hierarchical nature of an EDIF file.	6

UNIT - V

9	a.	Explain the goals and objectives of floor planning.	10
	b.	Describe various partitioning methods and mention the objective of partitioning.	10
10	a.	Write a short note on I/O and power planning of an ASIC system floor planning.	8
	b.	Explain timing-driven floor planning and placement design flow.	7
	c.	Write the steps followed in left-edge algorithm for local routing.	5

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