



P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

**First Semester, M. Tech. – Electronics and Communication Engineering
(VLSI Design and Embedded Systems)**

Semester End Examination; Jan/Feb - 2016

ASIC Design

Time: 3 hrs

Max. Marks: 100

Note: Answer FIVE full questions selecting ONE full question from each unit.

UNIT - I

- 1 a. What are the sequences of steps used to design an ASIC? Draw the flow diagram for the ASIC design. Also, comment on logical and physical design. 12
- b. Discuss are the advantages and disadvantages with the use FPGA and full custom ASIC. 8
- 2 a. What the different choices for using ASIC cell libraries? Briefly explain them. 6
- b. What does each ASIC cell contains when ASIC cell libraries are designed, explain each of them in detail. 10
- c. Define ASIC and give two examples for non – ASIC and ASICs. 4

UNIT - II

- 3 a. Construct a 16-bit carry select adder dividing into $M = 4$ blocks, with each block containing $P = 4$ adder cells in series. How do you obtain completion time T for the overall carry output signal? 8
- b. Recode the binary number $B = 00010111$ as CSD vector D . 6
- c. What are the ways to model capability of an I/O cell to withstand EOS? Explain them briefly. 6
- 4 a. Determine the optimum path delay for the logic cascade chain shown in Fig. Q 4(a). Also, compute the input capacitances C_2 , C_3 and C_4 . Ignore p and q of each stage. Given the logical ratio, $r = 2$, $C_1 = 1$ pF and $C_{out} = 5$ pF. 10

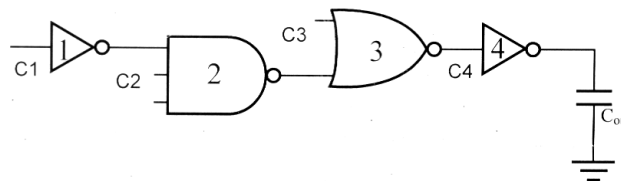


Fig. 4(a)

- b. Consider multistage AOI221 logic cell with each input driven by a minimum size inverter and the output inverter has IX drive strength, logic ratio = 1.5. 10
 $Z(A, B, C, D, E) = \text{NOT} (\text{NAND} (\text{NAND}(A,B), \text{AOI21}(C,D,E)))$

- i) Calculate the delay from input A to output Z.
- ii) Reduce the size of two NAND cells used in multi-cell implementation of an AOI221 without sacrificing speed.

UNIT - III

- 5 a. What is the need for hierarchical design? With suitable example explain the hierarchical design. Also explain how to label the nets in the hierarchical design. 11
- b. What are the difficulties of using ASIC schematic libraries? Briefly describe them. 4
- c. Name the two types of macros and programmable ASIC. Explain them. 5
- 6 a. What is netlist screener? List the errors that can be found by it and explain them. 12
- b. What you mean by Back-annotation? Explain in detail the need for it. 8

UNIT - IV

- 7 a. Illustrate how 2:1 MUX can be used as the function generator. 6
- b. Compare Actel ACT1, Xilinx XC3000, and Altera FLEX programming logic cells with respect to basic logic cell, logic cell contents, logic cell delay, interconnected delay, Flip – flop (FF) implementation. 9
- c. What are ways of optimization performed during logic synthesis? Describe them. 5
- 8 a. Describe with the help of block diagram the Xilinx XC4000 IOB. 8
- b. Write the hierarchical nature of an EDIF file. 4
- c. Explain the CFI connectivity model defined using Express – G language with an example. 8

UNIT - V

- 9 a. For the network graph, show in Fig. Q 9(b), apply KL algorithm to minimize the external edges. What are the problems or limitations of using KL algorithm for system partitioning? How can they be overcome?

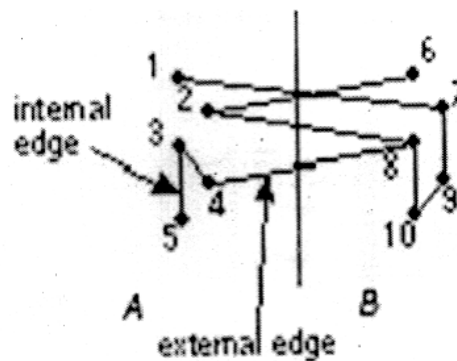


Fig. Q 9(b)

- b. What is the need of methods and algorithms in CAD tool designing? Briefly discuss the types of algorithms/functions used to reduce complexity. 8

- 10 a. Analyse the high tower area routing steps with an example. 5
- b. An ASIC chip has 40000 Flip-flops with input capacitance of clock input to each Flip-flop is 0.025 pF with clock frequency of 200 MHz, chip size of 20 mm on a side and clock spine consists of 200 lines across the chip with interconnect capacitances of 2 pF/cm and Vdd of 3.3 V, calculate : 5
- i) Number of stages to drive the clock spine.
 - ii) Power dissipated while charging the input capacitance of Flip-flop.
 - iii) Power dissipated while driving clock spine.
- c. Illustrate the different iterative placement improvement algorithm with examples. 10

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