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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Second Semester, M. Tech – VLSI Design and Embedded System (MECE)

Semester End Examination; June - 2016

Design of VLSI Systems

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1	a.	Clearly define description domains and levels of design abstraction.	6
	b.	Explain briefly the ACTEL Logic cell and ACTEL programmable I/O pad.	8
	c.	Explain briefly the SEA OF GATE and list the factors to keep the cost low.	6
2	a.	Describe different synthesis options available in chip design methods.	10
	b.	Write a note on EDA tools used in VLSI system.	10

UNIT - II

3	a.	Explain different types of simulation methods used in design verification tools.	10
	b.	Explain the following design capture tools in VLSI design : (i) HDL design (ii) Schematic design (iii) Layout design (iv) Floor planning.	10
4	a.	Explain 4-bit carry ripple adder using PG logic.	8
	b.	Write the schematic design of the 4-bit unsigned array multiplier.	8
	c.	Define black cell and gray cell.	4

UNIT - III

5	a.	With circuit diagram and implementation table, explain the operation of unsigned magnitude comparator.	8
	b.	Explain linear feedback shift register.	6
	c.	Explain array funnel shifter with schematic and stick diagram.	6
6	a.	Explain bit line conditioning and column circuitry used with respect to SRAM.	8
	b.	Explain with suitable diagrams, the operation of one transistor dynamic RAM cell.	8
	c.	Write a note on Queues in memory.	4

UNIT - IV

7	a.	What is FSM? Explain its types with figure. Why FSM is necessary in the design of control sub system?	6
	b.	Obtain the PLA implementation of one bit adder.	6
	c.	What are the properties of I/O sub systems? Explain the basic I/O pad circuits.	8

Contd…2

8 a. Explain the ideal properties of power distribution network. Also brief on,

(i) IR drop

(ii) $\frac{Ldi}{dt}$ drop. 10

b. Explain the generation of global clock with respect to PLL. 10

UNIT - V

9 a. Discuss the various components which accounts for non recurring engineering cost. 8

b. How schedule and person power are important in design economics? Explain. 6

c. Explain in detail, the built in self test technique of testing logic blocks. 6

10 a. Explain the state diagram of Test Access Port (TAP) controller. 10

b. Write a short notes on :

i) Stuck at faults 10

ii) IDDQ testing.

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