U.S.N | | | | | | | | | | |

P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, M. Tech – VLSI Design and Embedded System (MECE)

Make-up Examination; Jan/Feb - 2017

VLSI Testing and Verification

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Describe the faults in Digital Circuits. 10

b. Write short notes on :

i) Role of testing 10

ii) Digital and Analog VLSI testing.

2 a. Explain the following test generation techniques for combinational circuits :

i) One dimensional path sensitization 10

ii) Boolean difference.

b. Describe the detection of multiple faults in combinational logic circuits. 10

UNIT - II

3 a. Explain scan path technique for sequential circuits. 10

b. Describe ad-hoc design rules for improving testability. 10

4 a. Explain BIST architecture. 10

b. Explain the following :

i) Boundary scan 10

ii) Cross check.

UNIT - III

5 a. Develop a test algorithm for RAM. 10

b. Discuss the detection of pattern sensitive faults. 10

6 a. Describe reconvergence model with Human factors. 10

b. Write a note on : 10

i) Formal Verification ii) Functional Verification.

UNIT - IV

7 a. Explain lining tools and their limitations. 10

b. Write a note on : 10

i) Verification intellectual property ii) Hardware modelers.

Contd…2

8	a.	Explain the role of verification and various levels of verification.	10
	b.	Explain reusable components of verification, system level and board level verification.	10

UNIT - V

9	a.	Explain static timing analysis and its limitations.	10
	b.	Describe with a suitable diagram, linear and non-linear timing model with reference to VLSI design verification.	10
10a.		i) Compare cross tack glitch analysis and cross delay analysis.	5
		ii) Write a note on parasitic extraction.	5
	b.	Explain layout rule checks and electrical rule checks.	10

* * *