



P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, M. Tech – VLSI Design and Embedded System (MECE)

Semester End Examination; Dec - 16/Jan - 2017

VLSI Testing and Verification

Time: 3 hrs

Max. Marks: 100

Note: Answer FIVE full questions, selecting ONE full question from each unit.

UNIT - I

- | | | |
|------|--|----|
| 1 a. | Briefly discuss the VLSI technology trends affecting testing as complexity in the design increases. | 10 |
| | b. Describe bridging faults in digital circuits. | 4 |
| | c. Explain Digital and Analog VLSI testing in digital circuits. | 6 |
| 2 a. | List the fault models used in recent technology. Explain S-a-1 on one of the input of NAND ₂ gate. | 6 |
| | b. Discuss the effect of probable bridging fault in NOR ₂ gate with CMOS schematic and truth table. | 8 |
| | c. Realize $F = x_1x_2 + x_3x_4$ and find the Boolean difference with respect to x_3 . | 6 |

UNIT - II

- | | | |
|------|--|----|
| 3 a. | Explain the term controllability and observability with relevant diagrams. | 6 |
| | b. Analyze the clocked hazard free latches used in Level-Sensitive Scan Design (LSSD). | 10 |
| | c. Obtain the diagram of 4-bit LFSR for the polynomial $P(x) = x^3 + x + 1$ of degree 3. | 4 |
| 4 a. | Discuss the AD-HOC design rules to improve testability. | 4 |
| | b. Discuss the architecture of boundary scan. | 10 |
| | c. Realize the block diagram of circular flip flop using circular BIST architecture. | 6 |

UNIT - III

- | | | |
|------|--|----|
| 5 a. | Discuss the RAM organization with neat block diagram. | 12 |
| | b. Analyze the equivalence checking paths of 2 models employed in formal verification. | 8 |
| 6 a. | Explain the proposed BIST technique for testing embedded RAM with block diagram. | 12 |
| | b. Discuss the black-box and white-box functional verification approaches. | 8 |

UNIT - IV

- | | | |
|------|--|----|
| 7 a. | Analyze the behaviour of XOR gate using event-driven simulation when One i/p or Both i/p change. | 8 |
| | b. Along with flow diagram, explain levels of verification. | 12 |

- 8 a. Explain the cycle-base simulation employed for synchronous circuit. 8
- b. Discuss: 12
 - i) Hardware modules
 - ii) Verification intellectual property
 - iii) Waveform views.

UNIT - V

- 9 a. Explain the basic functionality of static timing analysis along with flow diagram. 10
- b. Analyze the min and max timing paths in clocking employed to EXOR gate. 6
- c. Briefly explain layout rule checks. 4
- 10 a. List out (any five) limitations of static timing analysis. 10
- b. Write a note on parasitic extraction. 4
- c. Briefly explain electrical rule checks. 6

* * *