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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

First Semester, M. Tech. - VLSI Design and Embedded Systems (MECE)

Make-up Examination; Feb -2017

Digital System Designing Using Verilog

Time: 3 hrs *Max. Marks: 100*

***Note**: i) Answer **FIVE** full questions selecting **ONE** full question from each unit.*
ii) Assume suitable missing data if any.

UNIT - I

1 a. Develop a sequential circuit with a single data input‘s’ and single data output ‘1’. The output is 1 when the input value in the current clock cycle is different from input value in the previous clock cycle. Describe also the timing diagram. 6

b. Explain the capacitive load and propagation delay. 4

c. Discuss the design methodology for an embedded system with block diagram. 10

2 a. Develop a verilog model for the burglar alarm to be priority encoder with zone 1 having highest priority zone 8 having lowest priority. 10

b. Explain axioms of Boolean Algebra and also prove the absorption laws using only the axioms. 10

UNIT - II

3 a. Develop a verilog model of a code converter to convert 4 bit gray code to 4 bit unsigned binary integer. 10

b. Describe IEEE standard 754 floating point formats. 10

4 a. Design a circuit for a modulo 10 counter and also develop a verilog model. 10

b. Explain clock synchronous timing methodology with relevant diagram. 10

UNIT - III

5 a. Explain multiport memories. Develop a verilog model of a dual port 4K x 16 bit flow through synchronous SRAM. One port allows data to be written and read while other port allows only data to be read. 8

b. Compute 12 bit ECC word corresponding to 8 bit data word 01100001. 4

c. Explain the difference between synchronous and asynchronous static RAM using timing diagram. 8

6 a. Describe I/O block of an FPGA with neat schematic. 6

b. Explain programmable array logic with example. 10

c. Describe differential signalling. How does it improve noise immunity? 4

Contd…..2

UNIT - IV

7	a.	Develop a verilog model to determine greater of Value-1 and Value-2.	10
	b.	Describe instruction encoding of Gumnut processor.	10
8	a.	Explain the working of 3 bit R string DAC.	8
	b.	Explain different serial interface standards.	12

UNIT - V

9	a.	Explain Kernel of an algorithm. If Kernel of an algorithm is accelerated by a factor of 100 and Kernel accounts for 90% of execution time before acceleration, what is overall speed up?	4
	b.	Describe briefly video edge detection using Sobel convolution mask. Write a Sobel edge detection algorithm.	8
	c.	Develop a verilog model for Sobel accelerates bus slave interface.	8
10	a.	Explain different optimization techniques in design methodology.	10
	b.	Discuss built in self test technique.	10

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