



P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester - M. Tech., VLSI Design and Embedded System (MECE)

Semester End Examination; Dec - 2016/Jan - 2017

Advances in VLSI Design

Time: 3 hrs

Max. Marks: 100

Note: Answer **FIVE** full questions, selecting **ONE** full question from each unit.

UNIT - I

- 1 a. What are the advantages of BICMOS technology over CMOS technology? 6
- b. Write the basic concept of MOS devices. Derive an expression for drain current in saturation and non-saturation regions of MOS devices. 8
- c. Derive an expression for MOS transistor, transconductance g_m and output conductance g_{ds} . 6
- 2 a. Derive an expression for the pinch-off voltage in a MESFET with an active layer thickness of t . 6
- b. Calculate the magnitude of saturation current in the following MESFET parameter. 6
Given: $N_d = 10^{17} \text{ cm}^{-3}$, $I_{D0} = 0.50 \text{ mA}$, $t = 0.1 \text{ } \mu\text{m}$, $K = 11.9(8.85 \times 10^{-14} \text{ F/cm})$, $V_g = 2\text{V}$.
- c. Describe the operation of MODFET (HMET) with energy band diagram. 8

UNIT - II

- 3 a. Discuss briefly small signal operation of MESFETs and MOSFETs with neat circuit model. 10
- b. Calculate the minimum capacitance for an n -channel MIS capacitor. Assume that the capacitor is made from Si-SiO₂-Al material systems. Given $N_a = 5 \times 10^{16} / \text{cm}^3$, oxide thickness $d = 12 \text{ nm}$, the insulator relative dielectric constant = 3.9 and the semiconductor relative dielectric constant is 11.8 and $n_i = 1 \times 10^{10} \text{ cm}^3$. 10
- 4 a. Explain in detail with suitable mathematical analysis of short channel effect on threshold voltage and surface mobility in a MOSFET. 12
- b. Explain the processing challenges to further CMOS miniaturization. 8

UNIT - III

- 5 a. Discuss briefly the cross section view of dual gate MOSFET devices. 6
- b. With a neat sketch, explain the working and construction of carbon nano tube FET. 10
- c. Discuss the advantages of molecular materials. 4
- 6 a. Explain the energy level diagram for molecular diode under all bias conditions. 10
- b. Describe the different aspects of conventional versus tactile computing. 10

UNIT - IV

- 7 a. Write the features of super buffers and explain the structure of NMOS schematic, stick diagram of, 10
i) Inverting super buffer ii) Non-inverting super buffer.

- b. Show that when an RC delay line is long, the signal delay tends to infinity and suggest means to improve the performance of the delay line. 10
- 8 a. Describe the salient features of pass transistor logic design, hence design two variables (A, B) pass transistor structure of, 7
- i) NAND ii) NOR.
- b. With a neat functional of general function block implement 2 input EXOR gate using N-MOS functional block. 7
- c. Discuss the dynamic ratio less inverters along with a neat diagram. 6

UNIT - V

- 9 a. Design the implementation of the following in both circuit and stick diagram, 10
- i) NAND-NAND implementation of $Y = ABC + DEF$
- ii) Static CMOS AOI technology of $Y = \overline{AB + CD}$.
- b. Explain the CMOS and NMOS implementation of 4 : 1 multiplexer with help of neat diagram. 10
- 10 a. Explain the term hierarchy, regularity, modularity and locality applied to IC's structured design. 10
- b. Write a short note on: 10
- i) Full custom design
- ii) Standard cell design.

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