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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Computer Science and Engineering

Semester End Examination; Dec - 2017/Jan - 2018

Digital Logic Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Realize the function $y = AB + \overline{C}$ using only (i) NAND gates and (ii) NOR gates. 8

b. Simplify the following function using Quine-McClusky method : 12

f(A B C D) = Σm(4, 8, 10, 11, 12, 15)+ d(9, 14).

2 a. Design a minimal hardware combinational circuit with 4 inputs A, B, C and D and 1 output Z, such that Z = 1 if numbers of 1's in the input is more than numbers of 0's, Z = 0 if numbers of 1's in input is less than numbers of 0's, Z = don't care when numbers of 1's is equal to numbers of 0's. 8

b. State and prove the following theorems with example : 10

i) Duality Theorem ii) Demorgon's Theorem.

c. Mention any two differences between positive logic and negative logic. 2

UNIT - II

3 a. Design and implement 2-bit magnitude comparator. 8

b. Implement full adder using 4 x 1 MUX. 6

c. Implement the following functions using 3 x 8 decoder : 6

$F_1(A, B, C) = \Sigma m(0, 2, 3, 5)$, $F_2(A, B, C) = \Sigma m(1, 2, 4, 7)$ and $F_3(A, B, C) = \Sigma m(1, 3, 6, 7)$.

4 a. Design and implement 4-bit carry look ahead adder. 10

b. Write a note on parity checker and parity generator circuit with example. 10

UNIT - III

5 a. Implement the following functions using PLA : 6

$F_1(A, B, C) = \Sigma m(0, 2, 4, 6)$, $F_2(A, B, C) = \Sigma m(1, 3, 5, 7)$ and $F_3(A, B, C) = \Sigma m(0, 1, 2, 3)$.

b. Give characteristic equations, state diagram and excitation table for : 12

(i) SR-flip flop (ii) JK-flip flop (iii) D-flip flop (iv) T-flip flop.

c. How do you convert JK-flip flop to T-flip flop? 2

6 a. Explain Edge triggered SR-Flip flop. 5

b. Explain Master-slave JK-flip flop. 8

c. Convert SR Flip- flop to JK-Flip flop. 7

Contd…2

UNIT - IV

7 a.	Design a synchronous counter using JK-flip flops to count the sequence: 0-2-4-6-0.	10
b.	Explain parallel in serial out shift register with circuit diagram, truth table and waveform.	10
8 a.	Briefly explain the design of Ring counter and Johnson counters using shift register.	10
b.	Design mod-6 synchronous counter using T-flip flop.	10

UNIT - V

9 a.	Explain Dual-slope A/D conversion.	10
b.	Write Verilog/ VHDL code to implement : (i) 8 x 1 MUX (ii) 3:8 decoder.	10
10 a.	Explain Binary ladder.	5
b.	Write VHDL code to implement : (i) 3 bit up counter and down counter (ii) Johnson Counter (iii) Ring Counter	15

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