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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Fifth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Dec - 2017/Jan - 2018

Digital CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Explain the formation of depletion region and inversion region in an n-channel enhancement type MOSFET along with cross section view and band diagram. 7

b. Discuss the constant voltage scaling technique and its effects on device performance. 6

c. Consider a simple P-N junction which is reverse biased with a voltage changes from 0 V to -5 V V_{bias}. The doping density of the N-type region is $N_D = 10^{19}\ cm^{-3}$. The doping density of the P-type region is $N_A = 10^{16}\ cm^{-3}$. The junction area is 20 µm X 20 µm. Calculate the average junction capacitance. 7

2 a. Write the circuit of resistive load inverter and explain the calculation of i) V_{DL} ii) V_{IL}. 7

b. Draw the circuit diagram of CMOS inverter and its VTC showing different regions of operation obtain the equation for threshold voltage of inverter. 7

c. For the depletion load inverter circuit with V_{DD} = 5 V, $V_{To,\ drives}$ = 1.0 V, $V_{T,\ o\ load}$ = -3 V, $\left(\frac{W}{L}\right)_{drives} = 2, \quad \left(\frac{W}{L}\right)_{load} = \frac{1}{3}$ 6

$K'_{n\ devices} = K'_{n\ load} = 25\ \mu A/V^2$, ϕ_F = -0.3 V, S

Substrate bias coefficient (γ) = 0.4 $V^{½}$. Calculate; i) V_{OH} ii) V_{OL}.

UNIT - II

3 a. Obtain the expression for high to low transition propagation delay for CMOS inverter using differential method. 7

b. A CMOS inverter with V_{DD} = 5 V, $V_{out} = V_{90\%}$ = 4.5 V, $V_{out} = V_{10\%}$ = 0.5 V, C_1 = 1 pf, $\mu_n C_{ox}$ = 20 µA/V^2, $(W/L)_n$ = 10, $V_{T,\ n}$ = 1.0 V. Calculate fall time τ_{fall} using average current method. 5

c. Explain the circuit and typical voltage waveform of 3-stage CMOS ring oscillator with identical inverters. Obtain equation for average propagation delay in terms of frequency. 8

4 a. Analyze the switching power dissipation of CMOS inverters along with related circuit diagram and waveforms also show that average power dissipation of CMOS inverter is proportional to the switching frequency. 8

b. Discuss the calculation of interconnect delay using RC delay model. 6

c. Explain the parasite capacitance and coupling capacitance effect of interconnect lines in IC. 6

Contd…2

UNIT - III

5 a. Write circuit of CMOS NAND 2 gate and obtain equation for threshold voltage V_{th} of the circuit in terms of K_n, K_p and $V_{DD.}$ 6

b. Write the CMOS schematic and stick diagram for NOR3 gate. 6

c. Explain the working of CMOS transmission gate with the bias condition and operating region and also obtain equation for equivalent resistance in different operating regions. 8

6 a. Explain the static behavior of two inverter basic bistable element with circuit schematic and voltage transformer curves. 6

b. Write the Gate level schematic and CMOS circuit based on NOR2 gate for SR latch and also explain the working of the circuit by designing the operating modes of the transistors in the circuit. 8

c. Discuss the operation of CMOS implementation of the D-latch and timing diagram. 6

UNIT - IV

7 a. Explain the logic '1' transfer and logic '0' transfers in NMOS dynamic logic with NMOS pass transistors with related circuit diagram and equations. 12

b. Analyze the charge storage and charge leakage phenomenon at a soft mode in a CMOS network. 8

8 a. Analyze dynamic voltage boots trapping arrangement to boost V_x during switching along with related equation. 10

b. Discuss the working of;

i) NP-Domino logic 10

ii) Zipper CMOS circuit.

UNIT - V

9 a. Analyze the operation of npn BJT operating in forward active mode and reverse active mode along with Ebers-moll equivalent circuit and equations. 10

b. Explain the working of BiCMOS inverter during transient output pull-up event and pull-down event along with equivalent circuit and equations. 10

10a. Define ESD and explain different models for ESD testing. 8

b. Explain the latch-up phenomenon in CMOS inverter with neat figure. 8

c. Write note on H-tree clock distribution technique. 4

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