U.S.N | | | | | | | | | |

P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Seventh Semester, B.E. - Electronics and Communication Engineering
Semester End Examination; Dec - 2017/Jan - 2018
Low Power VLSI Design

Time: 3 hrs   *Max. Marks: 100*

Note: Answer **FIVE** full questions, selecting **ONE** full question from each unit.

UNIT - I

1 a. What are the important needs for power optimization in VLSI system designs? What is the impact of technology advancement on power consumption? Explain.   10

 b. List the factors on which the short circuit energy of CMOS inverter depends. Obtain an expression for short circuit power dissipation in a CMOS inverter.   10

2 a. What are the sources of power dissipation? Explain.   10

 b. With a neat diagram, explain the energy band diagram for different biasing condition of MIS diode.   10

UNIT - II

3 a. What are the advantages of power optimization at behavioral level? Briefly explain different algorithmic level transforms for power optimization.   10

 b. Explain the following low design concepts :

   i) Architecture driven voltage scaling   10

   ii) Circuit activity driven architectural transformation.

4 a. Analyze the pre computation using Shannon's expansion with relevant diagrams.   10

 b. Explain the following low design concepts :

   i) Power optimization using operation reduction   10

   ii) Power optimization using operation substitution.

UNIT - III

5 a. Explain the transistor sizing and transistor reordering with respect to circuit level optimization.   12

 b. What are the different leakage currents encountered in a MOSFET device? Provide simple equations as applicable and suitable comments.   8

6 a. Explain the following clocked logic families and their role in low power designs :

   i) 2-inputs Domino logic NAND gate   ii) Pre-charge high DCSL.   6

 b. Implement the function using CMOS devices and briefly explain its working $y = \overline{(x_1 + x_2) x_3}$.   6

 c. Analyze the surface potential of short and long channel device at $V_c = 0$ V and $V_D > 0$ V.   8

UNIT - IV

7 a. Explain the principle of SSI CMOS inverter along with schematic and I-V characteristics. 8

b. Discuss the working of Self Adjusting Threshold Voltage Scheme (SATS) and DCVS type voltage level converter. 12

8 a. Analyze the designs with partially reversible logic with necessary example. 10

b. Discuss the generic resonant scheme for Adiabatic Dynamic Logic (ADL) inverter. 10

UNIT - V

9 a. What are the different levels available for power estimation through software design? Explain them briefly. 10

b. Analyze the performance of different edge types and for memory and register allocation constraints. 10

10 a. What are the different levels available for power optimization through software design? Explain them briefly. 10

b. Explain the sources of software power dissipation with example. 10

∗ ∗ ∗