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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Information Science and Engineering

Semester End Examination; Dec - 2017 / Jan - 2018

Computer Organization

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Explain the connection between the processor and memory of a computer with a neat diagram. 10

b. Briefly explain conditional codes with example. 6

c. Differentiate between CISC and RISC Instruction set. 4

2 a. With example, explain the following addressing nodes :

i) Register mode ii) Absolute mode iii) Immediate mode 10

iv) Indirect mode v) Index mode.

b. Explain the following in brief :

i) Processor clock ii) Basic performance equation iii) Pipe lining 10

iv) Clock rate v) Spec rating.

UNIT - II

3 a. Explain I/O parallel interface for an input device with a diagram. 8

b. Write a program that reads one line from keyboard, stores it in memory buffer and echoes it back to display. 8

c. Mention the sequence of events involved in interrupt handling. 4

4 a. What is Bus Arbitration? Explain two Bus Arbitration methods. 12

b. Explain all the available method to handle the interrupt requests from multiple devices. 8

UNIT - III

5 a. Explain internal organization of bit cells in a memory chip. 10

b. Explain set associative cache mapping technique. 10

6 a. With a neat diagram, explain how virtual memory address is translated to physical memory address? 10

b. Define the following terms with respect to cache memory :

i) Cache Hit/miss ii) Locality of reference iii) Dirty bit 10

iv) Write back v) Write through.

Contd…2

UNIT - IV

7	a.	Explain the design of sequential binary multiplier.	10
	b.	Write an algorithm for performing restoring division and compute 10101÷101.	10
8	a.	Describe the hardware implementation of floating point addition-subtraction unit.	12
	b.	Perform 14 × -7 using Booth's algorithm.	8

UNIT -V

9	a.	Explain the hard-wired control unit organization.	10
	b.	Explain the process of fetching a word from memory with example.	10
10	a.	Draw the flow chart for micro program of the instruction add src, rdst.	8
	b.	Show the three possible ways of implementing multiprocessor system with block diagram.	12

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