			Page No 1						
U.S.N									



P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Computer Science and Engineering Semester End Examination; Dec - 2017/Jan - 2018 Computer Organization

Time: 3 hrs Max. Marks: 100

Note: Answer FIVE full questions, selecting ONE full question from each unit.

UNIT - I

1	a.	Briefly discuss Big-endian and Little-endian Assignments. Give example.	5				
	b.	Explain different ways of Negative number representations. Give example.	6				
	c.	Define addressing mode. Explain any four addressing modes.	9				
2	a.	Explain the architectural connections between the processor and the memory.	8				
	b.	Explain different types of instructions capable of performing various types of operations.	8				
	c.	Using 5-bit representations, subtract the following numbers (-14) with (-8) using 2's complement method.	4				
		UNIT - II					
3	a.	Briefly discuss the working principle of the stack frame.	10				
	b. Explain different methods of vectored interrupt priority schemes.		10				
4	l a.	Give the general format of logical and arithmetic shift instructions. Explain with suitable examples.	10				
	b.	Explain various types of parameter passing with example.	10				
		UNIT - III					
5	a.	With neat figure, explain single bus organization of the data path inside a processor.	10				
	b.	What is bus arbitration? Explain the distributed arbitration scheme.	10				
6	a.	Explain control unit organization.	7				
	b.	Explain synchronous bus operation.	7				
	c.	c. Write the control sequence for execution of the instruction ADD (R3), R1.					
		UNIT - IV					
7	a.	Briefly explain the internal organization of a 2 Mx8 dynamic memory chip.	10				
	b.	b. With neat sketch, explain how the DMA controller registers that is accessed by the processor ar use of DMA controllers in a computer system.					
8	a.	Briefly discuss different types of ROM's.	10				
	b.	Write a note on: i) Hit rate ii) Miss penalty.	5				
	c.	Explain virtual memory address translation.	5				
		UNIT - V					
9	a.	Explain 4-bit carry-lookhead adder.	8				
	b. Explain different forms of IEEE standard for floating-point numbers.						
	c. Write an algorithml for nonstoring division.						
10	a.	. Briefly explain a logic circuit arrangement of restoring division also write an algorithm for the same.					
	h	Explain the hit main December of multiplians with a suitable example	10				

10

b. Explain the bit-pair Recording of multipliers with a suitable example.