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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Dec - 2017/Jan - 2018

Analog Electronics Circuits

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. With a neat diagram, explain the structure of *n*-channel enhancement type MOSFET. 6

b. Design the circuit shown in Fig. 1(b) to obtain a drain current of 80 µA. Find the value required for R, and find the DC voltage V_D, let the NMOS transistor have V_t = 0.6 V, $\mu_n C_{Ox}$ = 200 µA/V^2, L = 0.8 µm and w = 4 µm. (Assume λ = 0). 6

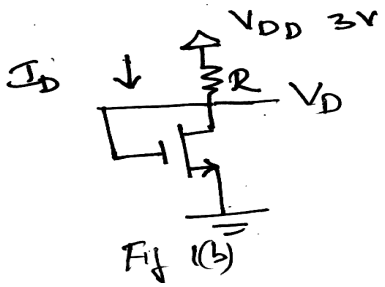

Fig 1(b)

c. Explain the working of MOSFET as an amplifier with the help of a neat diagram and the transfer characteristics. 8

2 a. With relevant diagram, explain biasing by fixing V_{GS}. 6

b. With the help of equivalent circuit and the simplified circuit, explain common source amplifier. 8

c. Design the circuit shown in Fig. 2(c) so that the transistor operates at I_D = 0.4 mA and V_D = +0.5 V. The NMOS transistor has V_t = 0.7 V, $\mu_n C_{ox}$ = 100 µA/V^2, L = 1µm and w = 32 µm. Neglect channel-length modulation effect (λ = 0). 6

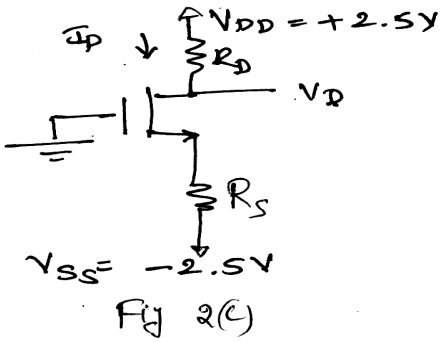

Fig 2(c)

UNIT - II

3 a. Define : 6

i) Input offset current ii) Slew rate iii) Input offset voltage.

b. Design a non-inverting amplifier to have a voltage gain of 66 for input amplitude of 15 mV by using Op-Amp741. (Assume I_{Bmax} = 500 nA). 6

Contd…2

c. Explain the operation of a difference amplifier with neat diagram and derive the equation for output voltage. 8

4 a. With a net diagram, explain the use of single polarity supply for capacitor-coupled voltage follower. 6

b. Design a capacitor-coupled voltage follower using a 741 operational amplifier. The lower cut-off frequency for the circuit is to be 50 Hz and the load resistance R_L = 3.9 kΩ. [Assume I_{Bmax} = 500 nA]. 6

c. With neat diagram, illustrate how high input impedance capacitor coupled voltage follower can be designed? 8

UNIT - III

5 a. With neat diagram, explain the phase lag compensation. 6

b. List precautions that should be observe for Op-Amp circuit stability. Explain in each case. 8

c. With the help of waveforms, explain the effect of slew rate on bandwidth and output amplitude. 6

6 a. With neat diagram, explain the working of non-inverting zero crossing detector. 6

b. With neat diagram, explain the working of integrating circuit. 6

c. Design a differenting circuit to give an output of 5 V, when the input changes by 1 V in a time of 100 µs. Use the Op-Amp with a bipolar input voltage. Draw the circuit diagram. 8

UNIT - IV

7 a. Explain the working of saturating precision half wave rectifier. 6

b. Show how a half wave precision rectifier can be combined with a summing circuit to produce a full wave precision rectifier. Explain. 8

c. Show how Zenor diodes can be used to limit the output. 6

8 a. Sketch an Op-Amp precision rectifier peak detector circuit. Explain the circuit operation. 6

b. Using a BIFET Op-Amp design an astable multi-vibrator to have a ±9 V output with a frequency of 1 kHz. Draw the circuit diagram. 7

c. Explain the working of 555 timer as an astable multi vibrator. 7

UNIT - V

9 a. Explain the working of phase shift oscillator. 6

b. Design a second order low pass filter for a cut-off frequency of 1 kHz. Draw the circuit diagram [use Op-Amp 741]. 6

c. With neat diagram, explain the working of triangular / rectangular wave generator. 8

10 a. With neat diagram, explain the working of adjustable output regulator. 8

b. Explain the working of 723 as low voltage regulator. 6

c. Design LM317 for an output voltage of 9 V. 6

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